10.2.2.4 VBAK

When the main VCC supply is off, the RAM and Real-Time Clock can be supplied a 3V data-retaining voltage from the VBAK regulator. It is a Linear (not switching) regulator, and derives power from either the Common Power Source, or from internal Lithium cells. If the voltage level of the Common Power Source is insufficient (for example, when the Battery pack is removed for replacement), then it derives power from the built-in rechargeable Lithium cells. It is the only load on these cells.

10.2.2.5 Lithium Charge

The lithium cells are constantly trickle-charged (when necessary) from the Common Power Source. The circuit is a Voltage-level Trickle charge circuit.

10.2.3 Hardware Level Detectors/Interrupts

To make battery level detection and warnings as automatic as possible, various fixed-voltage-level detectors are included. These are, specifically:

- SOURCE LOW (/SRCLOW)
- SOURCE DEAD (/SRCDEAD)
- POWERGOOD

There is also a two-color LED which is driven off these signals, to allow a visual indication of the power levels/warnings.

10.2.3.1 SOURCE LOW

SOURCE LOW is set to signal when the "common source" voltage level drops below 8.8V. It is wire-ORed with the real-time clock alarm and the "Power On" switch into the MFP Input 7, which is normally configured to generate an interrupt when the signal goes low. /SRCLOW, /RTC_ALARM, and /POWERON can all be read separately via the Configuration/Signal register; it is the only mechanism provided to distinguish the source of the interrupt.

10.2.3.2 SOURCE DEAD

SOURCE DEAD is set to signal when the "common source" voltage level drops below 7.2V. It generates a Level 7 (NMI) Interrupt when the signal transitions from high-to-low; the interrupt request is cleared and re-enabled upon vector fetch. This signal can also be read directly through the Configuration/Signal register.

10.2.3.3 POWERGOOD

POWERGOOD is purely a hardware-level "safety-valve", and cannot be read or controlled by software. It is set to trigger when the regulated VCC (+5V) signal drops to below 4.55V. If this occurs, /RESET is asserted and the hardware is signalled to turn the system off. If this occurs, the VCC, MOTOR, and LCD power convertors are all disabled, and the system automatically switches to low-voltage backup for the RAM and Real-Time Clock. The logic behind this "brute-force" approach is that system integrity cannot be guaranteed at VCC's below 4.55V, and protection of the RAMDISK (if present) is considered to be of highest priority.

10.2.3.4 Power LED

Power LED The Power LED is a two-color LED (Green and Red) which visually indicates the source level state of the machine. The Green segment is lit when POWERGOOD is active and /SRCDEAD is not; the Red segment is lit when /SRCLOW is active. Thus, the LED has four states:

OFF	When the STBook is turned off
GREEN	When the STBook is on and the Common Power Source is above 8.8V (i.e. power level is good)
YELLOW	When the STBook is on and the Common Power Source is between 8.8V and 7.2V (i.e. power level is low)
RED	When the STBook is on and the Common Power Source is below 7.2V (i.e. power is about to expire).

This last will rarely be actually seen, as it signals the operating system to do an emergency shutdown, which should take only a few milliseconds.

10.2.4 Software Control of Power Sources

Most of the power systems are under software control so that the operating system can keep power use as efficient as possible. These controls can also be used by applications to customize power usage for particular situations. While the exact registers and bits involved will be described later in this document, the system includes the ability to:

- Turn off the main VCC supply
- Turn on/off the Hard Disk motor supply
- Turn on/off the LCD Bias supply
- Turn on/off the RS-232 +/-9V generator
- Program the Real-Time Clock to turn on the main VCC supply.

10.2.4.1 Main VCC

The main VCC supply is controlled, in part, by a signal that, on a low-to-high transition of POWEROFF, turns it off. Since VCC drives all of the logic in the system, this also results in the Hard Disk and LCD Bias supplies being turned off, as well. It is recommended, however, that at least the LCD Bias be turned off before the main VCC is.

10.2.4.2 Hard Disk Motor Supply

The Motor supply is controlled directly by a signal MTR_PWR_ON, which must be high for the motor supply to be on. This signal is directly controlled by software. The intent of this control is two-fold:

To disable the switching regulator when it is known that the disk-drive motor is not spinning

To disable the motor when an attempt to spin-up the motor results in the power source level dropping too far.

10.2.4.3 LCD Bias

The LCD Bias supply is also controlled directly by software, in this case by the signal /22ON (the significance of this particular name is purely archaic). The intent of this control is, as previously stated, two-fold:

To sequence the voltages into the LCD circuitry properly.
To allow the system to save a bit of power when the system is not in use, by blanking the screen.

10.2.4.4 RS232 Drive

The RS232 drive level is not actually a separate power supply; rather, it is a pair of voltages generated by the RS232 interface IC. This generation can be disabled by software when it is known that the serial port is not in use, saving a small amount of power.

10.2.4.5 Real-Time Clock Alarm

The VCC supply can also be turned on by the Real-Time Clock Alarm, which is set under software control. Thus, it can be used to schedule operations for a later time/date, and the system can be turned off until that time.

10.2.5 User Input Signals and Controls

The user controls and influences the power state of the STBook through a variety of controls and switches. Some of the controls have different functions, depending on the current state of the STBook. The switches/controls are:

Power switch
Reset
"Top Closed"
Contrast

10.2.5.1 Power Switch

The Power switch is a momentary, push-button switch, located on the lower part of the top half of the STBook, at the lower left of the LCD screen. When the STBook is turned "off" (only the RAM and Real-Time Clock powered), it is used to turn the system on. Since the signal it generates is "wire-ORed" with the VCC POWERGOOD signal, one or the other must be present for the system to remain on. To the user, this means holding the Power Switch until the power LED turns either green or yellow, which indicates that VCC has reached its proper level; yellow indicates that the system is on, but the source level is low.

Pushing the Power Switch when the STBook is already on sends a signal to the software, indicating that the user wishes the system to be turned off. If the function is enabled, the software with take a "snapshot" of the hardware state at that time and save it in the RAM. Since all of the RAM contents are retained by the VBAK supply when the system is off, the "snapshot" can be used when the system is turned back on to return the system to exactly the state it was in when the system was turned off, even to the extent of returning to the application that was running at the time.

10.2.5.2 RESET

The reset signal is not, of course, really a power control; it is mentioned here for completeness. Its function is to reset the hardware and software state of the machine. It is also located at the lower left of the LCD display area, to the right of the Power Switch. It is deliberately recessed, so that it is unlikely to be pressed accidently.

10.2.5.3 Top Closed

The Top Closed switch is also not directly a power control; it is located between the Power Switch and the Reset Switch. The STBook housing is molded such that this switch is pressed when the top of the STBook is closed; this then generates a signal to the software, which can, for example, initiate the same power-down as the Power Switch. It also is used when the Real-Time Clock alarms turns on the system; the STBook then knows the top is closed, and that spinning-up the Hard drive would be inappropriate.

10.2.5.4 Contrast

The Contrast control is a potentiometer which allows the user to adjust the LCD Bias voltage level. Changing this level affects the LCD contrast; thus the user can set it to an appropriate level.

10.2.6 Power Source Level Direct Read

The current level of the Common Power Source can be read directly from an 8-bit A/D built into the STBook. It is designed such that each LSB change corresponds to 1/10V (100mV). Because of inaccuracies in the circuitry used, the built-in 2.5V reference level is converted at the same time as the Common Source level, and nominally converts to 1/2 full scale (i.e. 128 LSB's). This reference can then be used to scale the Power Source value; this is valid since the inaccuracies are only in the voltage ramp used to measure the levels; the scaling of the Common Source is done by 1% parts, and the reference is un-scaled. The level is read 2000 times/sec, and runs continuously while the VCC source is on.

10.2.7 Referenced Registers

This is a list of the specific registers and bits used to control all of the power system functions.

Address	Bit Positions	Register Name	Bit Name
FF 827E	0-5,7	LCD Control	
	Bit 0		Shadow Chip OFF
	Bit 1		/(SHIFTER OFF)
	Bit 2		POWEROFF
	Bit 3		/22ON
	Bit 4		RS-232_OFF
	Bit 5		(Unused in STBook)
	Bit 7		MTR_PWR_ON

Address	Bit Positions	Register Name	Bit Name
FF 9200	0-15	Configuration/ Signals	
	Bit 0		/(POWER_SWITCH)
	Bit 1		/(TOP_CLOSED)
	Bit 2		/(RTC_ALARM)
	Bit 3		/(SRCDEAD)
	Bit 4		/(SRCLOW)
	Bit 5		/(MODEM_WAKE)
	Bit 6		Reserved
	Bit 7		/(EXPANSION_WAKE)
	Bit 8		Reserved
	Bit 9		Reserved
	Bit 10		Reserved
	Bit 11		Reserved
	Bit 12		Reserved
	Bit 13		Self Test Bypass
	Bit 14		Low Speed Floppy
	Bit 15		DMA Available
FF 9210	0-7		Common Power Source Level Power Source Voltage Level
FF 9214	0-7		Reference Voltage Level Reference Voltage Level

Appendix A References

General

A Hitchhiker's Guide to the BIOS
Digital Research GEM Software Documentation

Main System

Motorola MC68HC000 16-Bit Microprocessor User's Manual, Fourth Edition
SGS-Thomson TS68HC901 Multi Function Peripheral Data Sheet

Graphics Subsystem

Adele Goldberg and David Robson, 'Smalltalk-80: The Language and Its Implementation', Addison-Wesley, Reading Massachusetts, 1983, Chapter 18.

Music Subsystem

General Instrument AY-3-8910 Programmable Sound Generator Data Sheet
MIDI Musical Instrument Digital Interface Specification 1.0

Device Subsystems

Atari Intelligent Keyboard (ikbd) Protocol and Specification
Hitachi HD6350 Asynchronous Communications Interface Adapter Data Sheet
Centronics Parallel Interface Specification
Electronic Industries Association RS232C Standard
Western Digital WD1770/1772 Floppy Disk Controller Data Sheet
Specification of the Atari Computer System Interface (ACSI)
Specification of the Atari Hard Disk Interface (AHDI)

Appendix B Notes

General

An address error occurs when a word instruction is used on a byte address.

Main System

The DMA Base Address and Counter Register must be loaded in low, mid, high order.

Graphics Subsystem

None.

Music Subsystem

The YM-3439 PSG I/O space and registers should be set up as critical regions in software.

Device Subsystems

Poll or service the Disk Drive Controller interrupt on the MK68901 MFP General Purpose I/O Register to detect the completion of a WD1772 FDC command. Do not poll the FDC Busy or DMA Sector Count Zero status bits.

Select the Sector Count Register before testing the DMA Status Register Error bit.

Do not set the 30 ms Settling Delay bit on WD1772 FDC type 2 and 3 command executions.

A force interrupt should be issued after a few seconds (ie timeout) on all commands sent to the WD1772 FDC.

Wait until the WD1772 FDC Motor On status is low before deselecting a floppy drive.

A floppy disk drive configuration table should be maintained in software to accommodate a diverse selection of 3.5 inch floppy disk drives. Two floppy disk drives currently under evaluation have the following characteristics:

500 Kbyte unformatted, 80 cylinders, one head, 3 ms stepping rate.
1 Mbyte unformatted, 80 cylinders, two heads, 3 ms stepping rate.