7.0 Memory Map

The first 2 Kbyte of STBook memory is reserved for the exception vector table and supervisor stack. This area along with I/O space is protected for supervisor references only. Accessing supervisor protected areas while in the user state will result in a bus error. A 4 word portion of ROM is shadowed at the start of RAM for the reset stack pointer and program counter. Writing to this area or any ROM location will also result in a bus error. The following is a map of STBook memory:

STBook Memory Map

00 0000	ROM	Reset: Supervisor Stack Pointer
00 0004	ROM	Reset: Program Counter
00 0008- 0F FFFF	RAM	1 Mbyte RAM
10 0008- 1F FFFF	RAM	1 Mbyte Shadow of 1st 1Mbyte (in 1 MByte machine), or 2nd MByte
20 0008- 3F FFFF	RAM	3rd & 4th Mbyte, in 4MByte machine
D4 0000- D7 FFFF	ROM	256K system extension ROM
E0 0000	ROM	Reset: Supervisor Stack Pointer
E0 0004	ROM	Reset: Program Counter
E0 0008- E7 FFFF	ROM	512K Base system ROM
E8 0000- EB FFFF	ROM	256K system extension ROM
F0 XXXX	IDE	IDE Drive Interface
FA XXXX	ROM	ROM Cartridge (128K total)
FB XXXX	ROM	
FF 8000	I/O	Configuration Registers
FF 8200	I/O	Display Registers
FF 8400	I/O	Reserved
FF 8600	I/O	DMA/Disk Registers
FF 8800	I/O	Sound Registers
FF 8A00	I/O	BLiTTER Registers
FF FA00	I/O	MC68XXX Registers
FF FC00	I/O	MC68XX Registers

8.0 I/O Map

The STBook I/O space ranges from FF 0000 to FF FFFF, with MC68HC000 and MC6800 peripheral internal registers starting at FF FA00 and FFFC00 respectively. Accessing reserved I/O addresses may result in a bus error. Bit values for various read and/or write registers are labeled as active One/_Zero (always mask out unused field bits).

The following is a map of STBook I/O space:

Address	R/W	Active Bits	Name
F0 xx00	R/W	0-16	DATA REGISTER
F0 xx04	R	1,2,4,6,7	ERROR REGISTER
		Bit 1	BBK Bad BlocK Detected
		Bit 2	UNC Uncorrectable Data Error
		Bit 4	IDNF ID field Not Found
		Bit 6	ABRT Command Aborted
		Bit 7	TK0 Track 0 not found
	W	0-7	WRITE PRECOMP REGISTER
F0 xx08	R/W	0-7	SECTOR COUNT
F0 xx0C	R/W	0-7	SECTOR NUMBER
F0 xx10	R/W	0-7	CYLINDER LOW
F0 xx14	R/W	0-7	CYLINDER HIGH
F0 xx18	R/W	0-4,7	SDH REGISTER
		Bit 0-3	Head Select Number
		Bit 4	Drive Select ("0" = Master, "1" = Slave)
		Bit 7	(Reserved)
F0 xx1C	R	0-7	STATUS REGISTER
		Bit 0	ERROR
		Bit 1	INDEX
		Bit 2	CORRECTED DATA
		Bit 3	DATA REQUEST
		Bit 4	DRIVE WRITE FAULT
		Bit 5	DRIVE SEEK COMPLETE
		Bit 6	DRIVE READY
		Bit 7	BUSY
	W	0-7	COMMAND REGISTER
F0 xx20	R/W	0-7	(UNUSED, RESERVED)
F0 xx24	R/W	0-7	(UNUSED, RESERVED)
F0 xx28	R/W	0-7	(UNUSED, RESERVED)
F0 xx2C	R/W	0-7	(UNUSED, RESERVED)
F0 xx30	R/W	0-7	(UNUSED, RESERVED)
F0 xx34	R/W	0-7	(UNUSED, RESERVED)

Address	R/W	Active Bits	Name
F0 xx38	R	0-7	ALTERNATE STATUS REGISTER
		Bit 0	ERROR
		Bit 1	INDEX
		Bit 2	CORRECTED DATA
		Bit 3	DATA REQUEST
		Bit 4	DRIVE WRITE FAULT
		Bit 5	DRIVE SEEK COMPLETE
		Bit 6	DRIVE READY
		Bit 7	BUSY
	W	1-2	DIGITAL OUTPUT REGISTER
		Bit 1	INTERRUPT ENABLE
		Bit 2	SOFTWARE RESET
F0 xx3C	R	0-6	DRIVE ADDRESS REGISTER
		Bit 0	/(DRIVE SELECT 0)
		Bit 1	/(DRIVE SELECT 1)
		Bits 2-5	/(HEAD SELECT)
		Bit 6	/(WRITE GATE)
	W	0-7	(UNUSED, RESERVED)
FF 8001	R/W	0-3	Memory Configuration
		----	Bank0 Bank1 (4MBytes)
		0000	Reserved
		0001	Reserved
		0010	Reserved
		0011	Reserved
		0100	Reserved
		0101	Reserved
		0110	Reserved
		0111	Reserved
		1000	Reserved
		1001	Reserved
		1010	2 Mbyte 2 Mbyte
		1011	Reserved
		11xx	Reserved
		[SEE STBook MEMORY SECTION]	
FF 8200	R/W	0-7	Video Base High
FF 8202	R/W	0-7	Video Base Low
FF 8204	R/W	0-5	Video Address Counter High
FF 8206	R/W		0-7 Video Address Counter Mid
FF 820	R/W	1-7	Video Address Counter Low
FF 820A	R/W	0-1	Sync Mode
		Bit 0	External/_Internal Sync
		Bit	150 Hz/_60 Hz Field Rate
FF 820C	R/W	1-7	Video Base (Low Byte)
FF 820E	R/W	0-7	Offset to next Line(Words)

Address	R/W	Active Bits	Name
FF 8240	R/W	0 Bit 0	Palette Color 0/0 (Border) Inverted/Normal Monochrome
FF 8260	R/W	0-1 00 01 10 11	Shift Mode Reserved Reserved 640 x 400, 1 Plane Reserved [SEE STBook VIDEO SECTION]
FF 8264	R/W	0-3	Horizontal Bit-Wise Scroll
FF 827E	W	0-7 Bit 0 Bit 1 Bit 2 Bit 3 Bit 4 Bit 5 Bit 6 Bit 7	LCD Control Shadow Chip OFF *SHFT output (Unused in STBook) POWER_OFF output (Turns off main VCC when HIGH) *LAMP output (turns off LCD Bias when HIGH) REFRESH_MACHINE output (turns on refresh controller) RS-232_OFF output (turns off +/- 10 generator) (Unused in STBook) MTR_POWER_ON (turns on IDE drive motor supply)
FF 8400 FF 8600 FF 8602		Reserved Reserved Reserved	
FF 8604	R/W	0-7	Disk Controller (Word Access)
FF 8606	R	0-2 Bit 0 Bit 1 Bit 2	DMA Status (Word Access) Error Status Sector Count Zero Status Data Request Inactive Status
FF 8606	W	1-8 Bit 1 Bit 2 Bit 3 Bit 4 Bit 5 Bit 6 Bit 7 Bit 8	DMA Mode Control (Word Access) A0 A1 HDC/_FDC Register Select Sector Count Register Select Reserved Disable/_Enable DMA FDC/_HDC Write/_Read
FF 8609 FF 860B FF 860D	R/W R/W R/W	0-7 0-7 0-7	DMA Base and Counter High DMA Base and Counter Mid DMA Base and Counter Low
FF 8800	R	0-7	PSG Read Data I/O Port B Parallel Interface Data

Address	R/W	Active Bits	Name
FF 8800	W	0-7	PSG Register Select
		Bits 0-3	Register Number
		0000	Channel A Fine Tune
		0001	Channel A Coarse Tune
		0010	Channel B Fine Tune
		0011	Channel B Coarse Tune
		0100	Channel C Fine Tune
		0101	Channel C Coarse Tune
		0110	Noise Generator Control
		0111	Mixer Control-I/O Enable
		1000	Channel A Amplitude
		1001	Channel B Amplitude
		1010	Channel C Amplitude
		1011	Envelope Period Fine Tune
		1100	Envelope Period Coarse Tune
		1101	I/O Port A (Output Only)
		1111	I/O Port B
FF 8802	W	0-7	PSG Write Data
		0-7	I/O Port A
		Bit 1	Floppy Side 0/_Side 1 Select
		Bit 2	Floppy _Drive 0 Select
		Bit 3	Floppy _Drive 1 Select
		Bit 4	RS232 Request To Send
		Bit 5	RS232 Data Terminal Ready
		Bit 6	Centronics _STROBE
		Bit 7	IDE RESET (Resets IDE drive interface; "wire-ORed" with system RESET into the interface)
			FDD_DENSE_SEL (selects High density [16MHZ clock] external Floppy)
		0-7	I/O Port Parallel Interface Data
FF 8A00		0-15	Halftone RAM
|			
FF 8A1E			
FF 8A20		1-15	Source X Increment
FF 8A22		1-15	Source Y Increment
FF 8A24		0-7	Source Address
FF 8A26		1-15	
FF 8A28		0-15	Endmask 1
FF 8A2A		0-15	Endmask 2
FF 8A2C		0-15	Endmask 3
FF 8A2E		1-15	Destination X Increment
FF 8A30		1-15	Destination Y Increment
FF 8A32		0-7	Destination Address
FF 8A34		1-15	
FF 8A36		0-15	X Count
FF 8A38		0-15	Y Count
FF 8A3A		0-1	HOP

Address	R/W	Active Bits	Name
FF 8A3B		0-3	OP
FF 8A3C		0-3,5-7	
		Bits 0-3	Line Number
		Bit 5	Smudge
		Bit 6	Hog
		Bit 7	Busy
FF 8A3D		0-3,6-7	
		Bits 0-3	Skew
		Bit 6	NFSR
		Bit 7	FXSR
FF 9200		8-15	Configuration Data
		Bit 0	/(POWER_SWITCH)
		Bit 1	/(TOP_CLOSED)
		Bit 2	/(RTC_ALARM)
		Bit 3	/(SOURCE_DEAD)
		Bit 4	/(SOURCE_LOW)
		Bit 5	/(MODEM_WAKE)
		Bit 6	(Reserved)
		Bit 7	/(EXPANSION_WAKE)
		Bit 8	
		Bit 9	Reserved
		Bit 10	Reserved
		Bit 11	Reserved
		Bit 12	Reserved
		Bit 13	SELF TEST
		Bit 14	LOW SPEED FLOPPY
		Bit 15	DMA AVAILABLE
FF 9210		0-7	Common Power Source Level Power Source Voltage Level
FF 9214		0-7	Reference Voltage Level
FF 9202		0-7	LCD Contrast control (Reserved for future use)
FF FA01		0-7	MFP General Purpose I/O
FF FA03		0-7	MFP Active Edge
FF FA05		0-7	MFP Data Direction
FF FA07		0-7	MFP Interrupt Enable A
FF FA09		0-7	MFP Interrupt Enable B
FF FA0B		0-7	MFP Interrupt Pending A
FF FA0D		0-7	MFP Interrupt Pending B
FF FA0F		0-7	MFP Interrupt In-Service A
FF FA11		0-7	MFP Interrupt In-Service B
FF FA13		0-7	MFP Interrupt Mask
FF FA15		0-7	MFP Interrupt Mask B
FF FA17		0-7	MFP Vector
FF FA19		0-7	MFP Timer A Control

Address	R/W	Active Bits	Name
FF FA1B		0-7	MFP Timer B Control
FF FA1D		0-7	MFP Timers C and D Control
FF FA1F		0-7	MFP Timer A Data
FF FA21		0-7	MFP Timer B Data
FF FA23		0-7	MFP Timer C Data
FF FA25		0-7	MFP Timer D Data
FF FA27		0-7	MFP Sync Character
FF FA29		0-7	MFP USART Control
FF FA2B		0-7	MFP Receiver Status
FF FA2D		0-7	MFP Transmitter Status
FF FA2F		0-7	MFP USART Data
FF FC00		0-7	Keyboard ACIA Control
FF FC02		0-7	Keyboard ACIA Data
FF FC04		0-7	MIDI ACIA Control
FF FC06		0-7	MIDI ACIA Data
FF FC20		0-3	Real Time Clock Seconds
FF FC22		0-3	Tens of Seconds
FF FC24		0-3	Minutes
FF FC26		0-3	Tens of Minutes
FF FC28		0-3	Hours
FF FC2A		0-3	Tens of Hours
FF FC2C		0-3	Day of Week
FF FC2E		0-3	Days
FF FC30		0-3	Tens of Days
FF FC32		0-3	Months
FF FC34		0-3	Tens of Month
FF FC36		0-3	Years
FF FC38		0-3	Tens of Years
FF FC3A		0-3	Mode
FF FC3C		0-3	Test
FF FC3E		0-3	Reset

The following tables list the STBook interrupt and signal priority assignments:

MC68HC000 Interrupt Autovector

Level	Definition
7	(HIGHEST)/POWER FAIL (NMI)
6	TS68HC901 MFP
5	(unused)
4	Vertical Sync (mid blanking)
3	(optional external)
2	Horizontal Sync (mid blanking)
1	(LOWEST)/(unused)

TS68HC901 Interrupt Control

Priority	Definition
15	(HIGHEST)/POWER_ALARMS/I7
14	RS232 Ring Indicator/I6
13	System Clock (Timer A)/TA
12	RS232 Receive Buffer Full/
11	RS232 Receive Error/
10	RS232 Transmit Buffer Empty/
9	RS232 Transmit Error/
8	Horizontal Blanking Counter (Timer B)/TB
7	Disk Drive Controller/I5
6	Keyboard and MIDI/I4
5	Timer C/TC
4	RS232 Baud Rate Generator (Timer D)/TD
3	BLiT Operation Done/I3
2	RS232 Clear To Send/I2
1	RS232 Data Carrier Detect/I1
0	(LOWEST)/Centronics BUSY/I0

NOTE: the IID6350 ACIA Interrupt Request status bit must be tested to differentiate between keyboard and MIDI interrupts.

10.0 Power Supply

10.1 Power Supply Specifications

An internal DC power supply provides power to the main system board and LCD. All power levels are regulated for over-voltage and over-current protection. The following are minimal power supply specifications:

VCC:

Input 8 to 20V
Output 5V +/-1%, 1A maximum steady-state; peaks to 3A

MTR:

Input 8 to 20V
Output 5V +/-1%, 1A maximum steady-state; peaks to 3A

LCD BIAS:

Input 8 to 20V
Output -12 to -17V (User adjustable), 50MA.

10.2 STBook Power Controls

The STBook incorporates a number of new sub-systems to allow tight control of the power usage of the machine. The operating system uses all of these to extend battery life of the machine; these functions will also be directly available to developers, so that they may customize the functions for any particular application. The various functions/topics are grouped as follows:

- Multiple Main Power Sources
- Multiple Regulated Power Outputs
- Software Control of the various Power Outputs
- Hardware Source Level Detectors/Interrupts
- User Input and Control Signals
- Power Source Level Direct Read
- Referenced Registers

10.2.1 Multiple Main Power Sources

The STBook can get its main power from various internal/external sources. These sources include:

- Replaceable battery pack (either NiCad or Alkaline)
- External AC adapter/charger, and internal rechargeable Lithium cells.

The first two are designed to run the machine in normal operation, and when "off" (i.e. only retaining the RAM contents and the Real-Time Clock, referred to herein as "back-up"); the last is only for back-up. The Battery Pack and AC Adapter supply power to a common point to feed to the various regulators; this point is henceforth referred to as the "Common Power Source."

10.2.1.1 Battery Pack

The battery packs available are an eight-cell Nicad pack, or a7-cell Alkaline pack. The Nicad pack can be charged from the AC adapter/charger while in the unit, and while the machine is in operation. A full charge should operate the machine for 5 to 10 hours, and should retain the RAM and Real-Time Clock for approximately 100 days; a new Alkaline pack, somewhat less.

10.2.1.2 AC Adapter/Charger

The supplied AC Adapter charger has input circuitry that automatically adjusts for 120/220V, 50/60Hz AC inputs, and both a Power and Recharge output. It is capable of fully recharging the NiCad cells in under two hours,while the machine is in use. It uses a "Delta-V Peak Detect" control circuit on the recharging output, to allow for the quick charge of the cells without overcharging them.

10.2.1.3 Lithium Cells

Under normal conditions, the small amount of power needed to retain the data in the RAM and to run the Real-Time Clock is derived from Common Power Source. If, for some reason, there is no power available from this source, power for the Back-up system is derived from the internal Lithium cells, which can maintain the RAM and RTC integrity for approximately 40 hours. The Back-up system also takes power from the Lithium cells when the Battery pack is being changed. When the Common Power Source is available, it recharges the Lithium cells.

10.2.2 Multiple Regulated Power Outputs

The STBook has various regulated power sources built in, all of which derive their power from the Common Power Source. These are:

- VCC (main 5V logic supply)
- MTR (5V supply for Hard Disk Motor)
- LCD BIAS (-15V generator for LCD contrast/bias)
- VBAK (3V backup for RAM and Real-Time Clock)
- Lithium Recharge

10.2.2.1 VCC

The main 5V logic supply comes from a switching regulator built-in to the STBook. It converts from the voltage level at the Common Power Source (AC adaptor, NiCad, or Alkaline) to the +5V needed for the logic. It is capable of supplying up to 1A @ 5V out with an input voltage as low as 8V. In includes current limiting on the input such that no more than 1.5A @ 5V is available at any input voltage, and short-circuit current is limited to 3A. The VCC regulator can be started by either the momentary-ON switch, or by the Real-Time Clock Alarm output. To stay on, the POWERGOOD level-detect circuit must be active before the turn-on signal is released. If at anytime the POWERGOOD signal fails, the VCC supply turns itself off.

10.2.2.2 MTR

The Hard Disk motor has a separate +5V supply, which also derives power from the Common Power Source. It is capable of supplying 1A @ 5V steady-state, and short peaks up to 3A. It does not have the level-detect circuitry that the VCC supply does; it is turned on/off by a software-controlled signal MTR_PWR_ON.

10.2.2.3 LCD BIAS

The LCD requires a bias voltage at a level between -12 and -16V. A third switching regulator creates this voltage, also from the Common Power Source. It has a user control (CONTRAST) that sets the actual voltage level. It can supply up to 50mA @ -16V. It does not have the level-detect circuitry of the VCC supply, and is turned on/off by a software-controlled switch, /22ON.