4.0 External Interfaces

The STBook supports five device subsystems:

- An intelligent keyboard
- Parallel interface
- RS232 interface
- MIDI interface
- DMA interface("Pseudo-ACSI").

Included with each device interface description is a port pin assignment chart with the STBook and programmable signals justified left [pins that are not connected are not shown]. The connector type on the STBook is shown above each pin list with an "S" designating a female socket and a "P" designating a male plug.

4.1 Intelligent Keyboard

The STBook has a socket to allow use an ST/Mega compatible keyboard. The Atari Intelligent Keyboard (ikbd) transmits encoded make/break key scancodes (with two key rollover), mouse/trackball data, joystick data, and time of day. The ikbd receives commands as well, with bidirectional communication controlled on the STBook side by an HD6350 Asynchronous Communications Interface Adapter supplied with transmit and receive clock inputs of 500 KHz. The data transfer rate is a constant 7812.5 bits/sec which can be generated by setting the ACIA Counter Divide Select to divide by 64. All ikbd functions such as key scanning, mouse tracking, command parsing, etc. are performed by a 1 MHz HD6301V1 8 bit Microcomputer Unit, in the keyboard.

4.2 Parallel Interface

The STBook parallel interface supports Centronics STROBE from the YM-3439 PSG for data synchronization and Centronics BUSY to the TS68HC901 MFP (ACKNLG is not supported) for handshaking. Eight bits of read/write data are handled through I/O Port B on the PSG at a typical data transfer rate of 4000 bytes/second.

Parallel Port Pin Assignments

STBook	DB 25S
PSG I/O A	1 Centronics STROBE
PSG I/O B	2 Data 0
PSG I/O B	3 Data 1
PSG I/O B	4 Data 2
PSG I/O B	5 Data 3
PSG I/O B	6 Data 4
PSG I/O B	7 Data 5
PSG I/O B	8 Data 6
PSG I/O B	9 Data 7
MFP	11 Centronics BUSY
	18-25 Ground

Signal Characteristics

Pin 1	TTL levels, active low.
Pins 2-9	TTL levels.
Pin 11	TTL levels, active high, 1 Kohm pullup resistor to +5 VDC.

4.3 RS232 Interface

The STBook RS232 interface provides voltage level synchronous or asynchronous serial communication. Five EIA RS232C handshake control signals are supported:

Request To Send and Data Terminal Ready are transmitted through the YM-3439 PSG I/O Port A

Clear To Send, Data Carrier Detect, and Ring Indicator are received through the MK68901 MFP.

The MFP USART transmit and receive clock inputs are controlled by the Baud Rate Generator MFP Timer D which is supplied with 2.4576 MHz and can support asynchronous data transfer rates from 50 to 19200 baud. One byte transmit and receive data buffers are managed by the MFP USART, which provides monitoring of buffer conditions and communication errors.

RS232 Port Pin Assignments

STBook	DB 9P
MFP	1 Data Carrier Detect
MFP	2 Received Data
MFP	3 Transmitted Data
PSG I/O A	4 Data Terminal Ready
	5 Protective Ground
	6
PSG I/O A	7 Request To Send
MFP	8 Clear To Send
MFP	9 Ring Indicator

Signal Characteristics

Pins 1-5,7-9 RS232C levels.

4.4 MIDI Interface

The STBook MIDI interface provides current loop asynchronous serial communication controlled by an HD6350 ACIA supplied with transmit and receive clock inputs of 500 KHz. The data transfer rate is a constant 31.25 Kbaud which can be generated by setting the ACIA Counter Divide Select to divide by 16. The MIDI specification calls for serial data to consist of eight data bits preceded by a start bit and followed by one stop bit.

MIDI Port Pin Assignments

MIDI OUT/THRU

STBook	Circular Mini-DIN 5S
MIDI IN	1 THRU Transmit Data
	2 Shield Ground
	3 THRU Loop Return
MIDI ACIA	4 OUT Transmit Data
	5 OUT Loop Return

MIDI IN

STBook	Circular Mini-DIN 5S
MIDI ACIA	4 IN Receive Data
	5 IN Loop Return

Signal Characteristics

Current Loop 5 ma, zero is current on.

4.5 DMA Interface (Pseudo-ACSI)

The DMA interface on the STBook, while incorporating more signals than the Atari standard ACSI interface, is not intended to expand the existing definition of ACSI. The extra signals are, rather, added to allow the Floppy Disk controller chip (WD 1772) to be located external to the STBook; hence, the name Pseudo-ACSI. These include the "adapter voltage", which is just the power coming in from an external AC adapter, allowing the external floppy to be AC powered when the STBook is. Note that this means conversion from Pseudo-ACSI to ACSI is merely a cable which connects the ACSI signals to the appropriate points on the Pseudo-ACSI port; no active electronics are required.

The new signals are, in no particular order: AVLTG, FDINT, D1SEL, D0SEL, S0SEL, FDRQ, /FDCS, FDD_DENSE_SEL. The first is, as mentioned before, the voltage from the AC adapter; the last is the only truly "new"signal. It was added so that an external floppy drive can use either normal or high density floppy disks, by changing the "CLK" signal into the WD 1772. By definition, FDD_DENSE_SEL "low" indicates use of an 8MHz clock into the 1772 (low density), and FDD_DENSE_SEL "high" indicates use of a 16MHz clock (high density).

The other signals are simply those that were purely internal to previous STE designs: /FDCS is the chip select for the 1772; FDRQ is the data-request from the 1772; FDINT is the interrupt-request from the 1772. D0SEL selects the drive chosen to be the equivalent to the previously "internal" or "A" drive; D1SEL selects the drive chosen to be the equivalent to the previously "external" or "B" drive. S0SEL selects the active side for whichever drive is selected.

Pseudo-ACSI Port Pin Assignments

STBook	Micro-D 28S	(ACSI Equivalent)
AVLTG	1 adapter Voltage	
AVLTG	2 adapter Voltage	
AVLTG	3 adapter Voltage	
FDD_DENSE_SEL	4	
/RESET	5	12
/HDINT	6	10
FDINT	7	
D1SEL	8	
D0SEL	9	
S0SEL	10	
/HDRQ	11	19
/HDCS	12	9
FDRQ	13	
/FDCS	14	
CR/W	15	18
/ACK	16	14
CA2	17	
CA1	18	16
CD7	19	8
CD6	20	7
CD5	21	6
CD4	22	5
CD3	23	4
CD2	24	3
CD1	25	2
CD0	26	1
GND	27 Ground	17,15,13,11
GND	28 Ground	17,15,13,11

5.0 Components

The standard configurations of the Atari STBook main system, graphics subsystem, music subsystem, and device subsystems are made up of the following major hardware components:

Main

- 8 MHz MC68HC000 Microprocessor Unit
- TS68HC901 Multi Function Peripheral
- 256 Kbyte System ROM
- 1 or 4 Mbyte RAM
- COMBO IC
  - Memory Controller
  - Control Logic
  - BLiTTER

Graphics

- 32 Kbyte Display Memory (from main RAM)
- LCD SHADOW Controller Chip
- 640x400 0.27mm pitch LCD panel

Music

- YM-3439 Programmable Sound Generator

Device

- Atari Intelligent Keyboard (ikbd) connector
- 2 HD6350 Asynchronous Communications Interface Adapters

6.0 STBook/STylus Expansion Bus

6.1 Electrical Specification

6.1.1 Power Available

External devices must not draw more than 400mA total from VCC on the connector.

6.1.2 Loading

External devices must not present more than a total of 1 (one) LS-TTL load per line onto the signals; open-collector drivers should be prepared to sink 20mA, on those lines which require it, such as EXPANSION_WAKE-.

6.2 Signal Descriptions

The Atari STBook can be expanded externally using the 120-pin expansion bus, which is new to the STylus and STBook machines. It essentially allows direct access to the 68HC000 address and data buses, and bus control signals to allow appropriate response. There are also the XROM3 and XROM4 signals to allow for conversion to the previous "ROM Cartridge" format without the need for active electronics (i.e. a 120-pin expansion to 40-pin ROM cartridge convertor would consist of two connectors and a PCB).

The following signals are all direct from the 68HC000, and need no special description:

A1-A23	Address Lines
D0-D15	Data Lines
AS-	Address Strobe
LDS-/UDS-	Lower/Upper Data Strobes
R/W	Read/Write Control
FC0-FC2	Function Code 0-2
VPA-	Valid Peripheral Address
VMA-	Valid Memory Address
E	"E" clock
RESET-	Reset signal
HALT-	Halt signal

Two signals are also direct from the 68HC000, but require a bit more operational detail:

DTACK-	Data Transfer Acknowledge
BERR-	Bus Error

The "Glue" chip uses DTACK- to acknowledge memory spaces it controls; it "Bus Errors" on other spaces (or "illegal" access to valid spaces) by not generating DTACK-. Other circuitry in the "Glue" chip times the length of the AS- signal; if it is longer than 8uS, than BERR- is asserted. What this means is that a device on the 120-pin expansion bus can be logically located in address spaces that the "Glue" chip considers "illegal"; all that is necessary is to generate a DTACK- early enough such that AS- does not extend to 8uS.

Two signals are simply the outputs generated by the Glue chip for particular memory spaces, specifically those for the ROM cartridge space. Because the Glue assumes these are ROMs, only reads of this space are acknowledged or selected by the Glue chip. A third signal, DEV-, simply indicates when a peripheral address has been selected in supervisor mode; DTACK- is not necessarily asserted.

There is also DMA-, which indicates that a Floppy or ACSI DMA cycle is occurring. It is included because the COMBO/Glue chip, while asserting AS- and L/UDS-, leaves the address bus in a high-impedance state. Because of the high value pull-up resistors used in the STBook and STylus, the address lines may rise quite slowly when the lines are left in high-impedance. Noise could couple in, and false addresses could be asserted (this problem arose, for example, in the IDE interface circuitry in the STBook). It is therefore recommended that any address decoding added to the STBook or STylus use DMA- as an additional (active HIGH) qualifier.

ROM3-
ROM4-
DEV-
DMA-

Use of the Bus Grant system is possible, with some limitations. While the Bus Request and Bus Grant Acknowledge are direct connections to the 68HC000, the Bus Grant signal is an output from the Glue chip. This means that the Glue chip (which includes the Blitter and DMA control) has priority for the gaining control of the Bus; Bus Grant is passed through only if no request is pending internal to the Glue.

BR-	Bus Request
BGACK-	Bus Grant Acknowledge
MCUBG-	Bus Grant, out from the Glue chip.
CPUBG-	Bus Grant, from the CPU to the Glue chip (this is for reference only)

Some interrupt control is also possible, at two separate priority levels. One is a level 3 interrupt, for which an input into the Glue chip priority encoder is provided. For this level, it is the responsibility of the external circuit to respond to the interrupt acknowledge cycle, and to provide a method to clear the interrupt request. Both Auto-Vector and Vectored interrupts are possible.

The external circuitry can also share the Level 6 interrupt with the 68HC901 MFP internal to the STylus and STBook. The external interrupt source can have either higher or (preferably) lower priority than the internal MFP. All of this is accomplished three signals: MFPINT-, MFPIEI-, MFPIEO-.

The first is a open-collector driven, wire-OR signal, indicating a level 6 interrupt. The next two establish the relative priority of the two interrupt sources. MFPIEI- (MFP Interrupt Enable In) signals the MFP that no higher priority device is requesting the interrupt service (active LOW, internal pull-down). MFPIEO- signals that the MFP has no pending interrupts, and that MFPIEI-is active; i.e. no higher priority interrupt is pending. Thus, a multi-level structure can be obtained. Because many internal functions depend on the level 6 interrupts of the MFP, we recommend that external devices install themselves at a lower level, but do not require it.

The relevant signals for interrupt control are:

EINT3-
MFPIEI-
MFPIEO-
MFPINT-
IPL0-, IPL1-, IPL2-
IACK-

To help in synchronization of external circuits (particularly when the Refresh Machine described above is running), a small number of clock signals are provided. They are:

CLK16	Main 16MHz clock
CLK8	Above clock /2; CPU clock
KHZ500	Above clock /16; Baud Rate Clock

Finally, some power and power control signals are provided to allow external devices to draw some power from the VCC supply of the STylus or STBook. Because of internal demands and limits, we require that external devices draw no more than 500mA from this port. To help distribute the power evenly, and to help maintain clean logic levels, there are 10 VCC signals, and 30 GROUND signals. 10 of the GROUND signals are located at the ends of the connector, opposite the VCC signals; the other 20 are distributed as every 5th pair of signals across the connector. This should aid in both maintaining a clean ground, and reducing EMI.

Power Control is possible to some degree using the signal EXPANSION_WAKE-. This signal expects to be driven by an open-collector driver; when pulled to ground, this "powers on" the STylus/STBook. It is equivalent to pressing the "Power" button on either machine; it's current state can be read from the Configuration/Switch register.

And finally, there is a pin which allows a peripheral plugged into the STBook or STylus to determine which it is connected to. Pin 94 is defined to be a no-connect on an STBook, and grounded on a STylus. The peripheral could, conceivably, determine the type of host without the host being powered; this is the responsibility of the peripheral, if it needs to know it.

The Expansion connector has the following pin assignments:

Expansion Port Pin Assignments

Micro-D 120S

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VCC	2	VCC	3	VCC	4	VCC
5	VCC	6	D0	7	D2	8	D4
9	D6	10	GND	11	D8	12	D10
13	D12	14	D14	15	GND	16	NC
17	A2	18	A4	19	A6	20	GND
21	A8	22	A10	23	A12	24	A14
25	GND	26	A16	27	A18	28	A20
29	A22	30	GND	31	/HALT	32	/VMA
33	/BR	34	/BGACK	35	GND	36	FC0
37	FC2	38	R/W	39	UDS	40	GND
41	/RESET	42	/IPL0	43	/IPL2	44	EXPANSION_WAKE-
45	GND	46	/MFPINT	47	/EINT3	48	/DMA
49	/ROM3	50	GND	51	NC	52	NC
53	CLK16	54	KHZ500	55	GND	56	VCC
57	VCC	58	VCC	59	VCC	60	VCC
61	GND	62	GND	63	GND	64	GND
65	GND	66	D1	67	D3	68	D5
69	D7	70	GND	71	D9	72	D11
73	D13	74	D15	75	GND	76	A1
77	A3	78	A5	79	A7	80	GND
81	A9	82	A11	83	A13	84	A15
85	GND	86	A17	87	A19	88	A21
89	A23	90	GND	91	/STylus	92	/CPUBG
93	/MCUBG	94	NC	95	GND	96	FC1
97	/AS	98	/LDS	99	/DTACK	100	GND
101	/VPA	102	/IPL1	103	/IACK	104	/BERR
105	GND	106	/MFPIEI	107	/MFPIEO	108	/DEV
109	/ROM4	110	GND	111	NC	112	NC
113	CLK8	114	E	115	GND	116	GND
117	GND	118	GND	119	GND	120	GND