FEATURES

- Provides hardware assist for bit-mapped graphics operations. Includes 32-bit barrel shifter
- Performance increase over software implementations:
  - –Monochrome = 4 x Software
  - –Color = 4 x (Planes) x Software
- Supports both CRT displays and such hardcopy devices as laser printers
- Compatible with both monochrome and color displays
- Implements all 256 possible raster operations on source, destination, and pattern data
- 28- pin package; 5 V supply

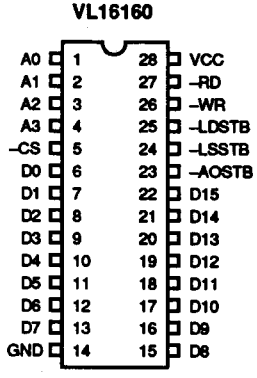
DESCRIPTION

The VL16160 Raster Op ALU (RALU) provides hardware-assisted performance enhancements for bit manipulation operations used in bit-mapped graphics displays. These operations, called bit block translation (BITBLT), allow bit-mapped images to be combined and manipulated by logical operators. These operators include AND, OR, and XOR, and can be used on source, destination, and pattern data. Additionally, support for masking with multiple mask registers for clipping is included.

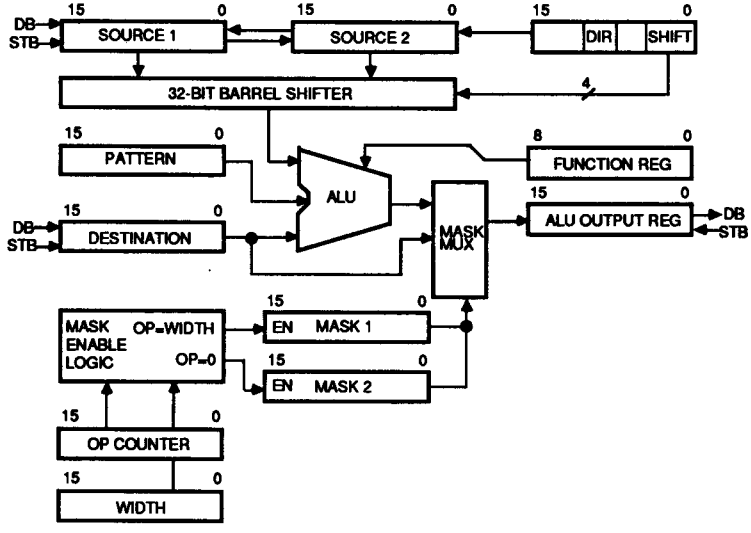
The BITBLT operation is general purpose enough to be used in a wide range of graphics operations, including text display using arbitrary fonts, attributes, and enhancements. Successive applications of BITBLT can perform such operations as scaling, filling, rotations, and texturing.

In a typical application, the RALU operates on display data in 16-bit words that are latched into its input buffers by external hardware. Once source, destination, pattern, shift, and masking data are loaded into the RALU, the source data is bit-aligned with the destination data, and the logical operation specified in the function register takes place. The results are stored in the ALU Output Register, which can be output onto the bus by a single strobe signal.

PIN DIAGRAM



BLOCK DIAGRAM



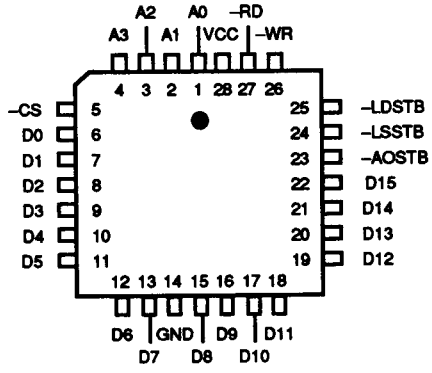
ORDER INFORMATION

Part Number	Package
VL16160PC	Plastic DIP
VL16160CC	Ceramic DIP
VL16160QC	Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

PIN DIAGRAM

VL16160-QC



SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
D0-D15	6-15	Bidirectional data lines; input enabled by –CS and –WR. Input data to Destination Register must be stable relative to the trailing edge of –LDSTB. Output enabled by –CS, –RD, and A0-A3 or –AOSTB.
–CS	5	Chip Select; Must be active to write to or read from internal registers.
–RD	27	Read Enable; Input used to strobe any internal register data to the data bus pins. Must be active in conjunction with –CS.
–WR	26	Write Enable; Input used to strobe data on data bus pins into the selected register. Must be active in conjunction with –CS.
A0-A3	1-4	Register Address; Address inputs that specify the internal chip register to be accessed for a read or write operation.
–AOSTB	24	ALU Output Strobe; Input used to enable the output of the function decoder onto the data bus pins. Cannot be active when –CS and –RD or –WR are active.
–LDSTB	25	Load Destination Register Strobe; Input used to strobe the value (address) on the data bus pins into the Destination Register. Value on A0-A3 need not be valid when –LDSTB is used to load the Destination Register. The –LDSTB pin also decrements the op counter each time it is pulsed.
–LSSTB	24	Load Source Register Strobe; Input used to strobe the value on the data bus into the Source Register specified by the Direction Bit. The other Source Register is loaded with the previous contents of the Source Register being loaded.
GND	14	Ground
VCC	28	+5 V ± 5%

FUNCTIONAL DESCRIPTION

The VL16160 consists of four basic blocks: Source Shifter, Function Decoder, Op Counter, and the Register set. The internal data bus is 16 bits wide, enabling all internal registers to be accessed easily from the I/O bus for context saving and restoring. In operation, the Source Shifter extracts data from the Source Registers and shifts the data to be aligned with the data in the Destination and Pattern Registers. The Function Decoder then performs a 16-bit Boolean operation as specified by the Function Register with the data extracted from the Source Registers and the data in the Destination and Pattern Registers. The result of the Boolean operation is available on the external I/O bus when the –AOSTB signal is strobed and can easily be written back into display memory. The Op counter and associated registers provide the support for clipping operations as required by the application.

SOURCE SHIFTER

The Source Shifter performs bit alignment on the concatenated 32 bits of data in the Source 1 and Source 2 Registers. The amount of bit alignment performed is based upon the value in the Shift Value Register. When –LSSTB is strobed, the Source Shifter extracts 16 contiguous bits from the 32 bits of data in the Source 1 and Source 2 registers as follows:

1. If the low order four bits of the Shift Value Register have a non-zero value, that value specifies the shift count by which the 16-bit field to be extracted is offset from bit 0 of the concatenated source registers, as shown in Figure 1. The result is passed on to the Function Decoder.
2. If the low-order four bits of the Shift Value Register is 0, the contents of either Source 1 or Source 2 are passed directly to the Function Decoder and no shifting occurs. The direction bit indicates which source register is used in the operation, as shown in Figure 1.

FUNCTION DECODER

The Function Decoder performs a Boolean operation on the contents of the Destination Register, Pattern Register, and the output of Source Shifter. The Boolean operation is specified by the Function Register. With the three operands, 256 different Boolean operations are possible. The result of the operation is available on the I/O bus when the –AOSTB control signal is active. –AOSTB signal cannot be active at the same time that –CS and –RD or –WR are active. The result of the Boolean operation is also available by reading the ALU Output Register.

To understand how the Function Decoder performs the desired Boolean operation, note again that with three operands, (data in the Source, Pattern and Destination Registers), a total of 256 different boolean operations is possible. Out of these 256 possible operations, the application defines which are needed to perform the desired task.

For example (see Figure 2), to "paint" a new image over an existing image requires the source data (image) to be ORed with the destination data (image). This means "Source Register OR the Destination Register". For each bit, there are four possible results of this operation between these two registers. However, since the Pattern Register is always included, even when it is a "don't care," a total of eight different possible results of this one Boolean operation is possible. These eight combinations define the "function code" for the overlay operation. Thus, the function code is really defined as the result (and the only result possible) of a Boolean combination of the Source, Destination, and Pattern Registers. In using the VL16160, the application defines which of the 256 possible Boolean combinations of the Source, Destination and Pattern Registers define those "functions" required of the application, and when that "function" is required, the corresponding function code is loaded into the Function Register.

In principal, the Function Decoder operates on a bit-by-bit basis as a 1-of-8 data selector with each data bit in the Source, Destination, and Pattern Registers selecting one of eight bits of data from the Function Register.

The function codes required of an application are determined ahead of time by the user and stored in memory to be used as needed. The determination of the correct function code is a matter of simply applying the definitions stated above (see Figure 2), in a simple method. The truth table for Pattern, Source, and Destination bits is written, with the desired output. This desired output is read as the desired value of the Function Register, with the least significant bit as shown in Figure 2. Using this method, the software engineer can easily define a pattern to suit each specific need.

OP COUNTER

The Op Counter, in conjunction with the Width and Mask Registers, provides for masking of selected bits in the Destination Register. This masking prevents the VL16160 from modifying selected areas of display memory when performing BITBLTs. For example, clipping may be required at the edges of a window. The function of the Op Counter is to keep track of the beginning and end of each row, so that the mask registers can handle this clipping automatically, without additional processor intervention.

The Op Counter must be correctly initialized prior to the beginning of a raster operation. The enabling of masking is internally clocked by the –LDSTB signal. For this reason, after loading the Op counter with an initial value, –LDSTB must be pulsed before the –LSSTB of the first operation. Since this –LDSTB will decrement the Op Counter, it is necessary to increment the Op Counter to be one more than the intended value, so that this "dummy" –LDSTB starts out the BITBLT with the correct Op Counter value. This "dummy" –LDSTB does have to be repeated between scanlines, as the masking remains enabled. If context switching is utilized, however, reinitialization (with the loading of Op Counter and subsequent –LDSTB) is necessary before leaving a context, or upon re-entering one, in the middle of a BITBLT.

REGISTER DESCRIPTION

As shown in the block diagram, the RALU consists of a number of registers, each connected to the internal 16-bit data path. Of these registers, three are used very often and are directly accessible from the data bus by the assertion of strobe signals.

SOURCE
The Source Register holds a 16-bit word of data to be modified by a raster operation. It is loaded from the data bus by the assertion of the –LSSTB signal.

DESTINATION
The Destination Register holds a word of data from the bit-mapped display that is modified by the source data and raster operation. It is loaded from the data bus when –LDSTB is asserted.

ALU OUTPUT
The ALU Output Register holds the result of the raster operation to be written back to memory. The contents may be put onto the data bus by the assertion of the –AOSTB signal.

The remainder of the registers are typically set up for a series of operations and are not changed until the end of a scan line.

DIR / SHIFT
This register controls the direction of the raster operation (left-to-right or right-to-left). In addition, it specifies the number of bits to shift to align the source with the destination fields.

MASK 1 and 2
These registers are used to define the left and right boundaries of the area on the screen that is manipulated. (The direction bit affects which register corresponds to left vs. right). A bit set in these registers allows the corresponding bit in the Destination Register to pass through unaltered. When the Op Counter is equal to the Width Register (usually for the first raster operation on each scan line), the Mask 1 Register selects bits to be included in the operation. Masking is disabled until the Op Counter is zero (usually for the last operation on a scan line); at that time, the Mask 2 register is used.

PATTERN
This register contains data to be combined with the output of the bit-shifted source register. This is commonly used for enhancing an image with a background pattern.

FUNCTION
This register contains the operator that is used to combine the source, destination, and pattern data.

OP COUNTER
The Op Counter Register specifies the current count of the operation in progress. The Op Counter is decremented each time –LDSTB is brought active. After the Op counter goes to zero, the next –LDSTB causes the Op counter to be reloaded with the value of the Width register prior to the next operation. The Op counter can be set to the value of the Width Register at the start of a raster operation by beginning an operation with a "dummy" –LDSTB. This loads the Op counter in preparation for the first scan line.

WIDTH
The Width Register specifies the width of the line (in 16-bit words) on which raster operations will take place.

FLAG REGISTER
The Flag Register is uncommitted and can be used to temporarily store context information for multi-tasking implementations.

FIGURE 1. SHIFTING AND DIRECTION

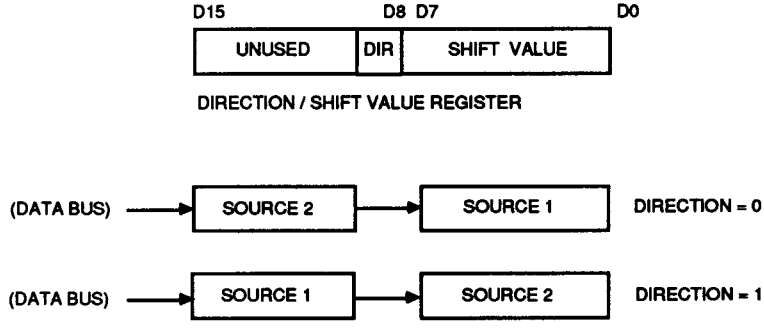


TABLE 1. REGISTER MAP

0	Destination Register
1	Source 1 Register
2	Source 2 Register
3	Pattern Register
4	Mask 1 Register
5	Mask 2 Register
6	Shift Value Register
7	Function Register
8	Width Register
9	Operation Count Register
10	ALU Output Register
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Flag Register

FIGURE 2. RASTER OPERATIONS EXAMPLE

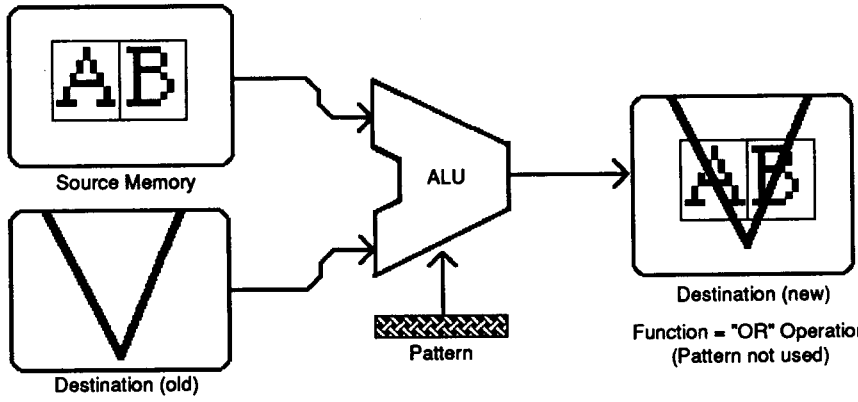


FIGURE 2a. SOURCE XOR DESTINATION (66_{16})

Pattern	Source	Dest.	Funct.
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

MSB

LSB

Example

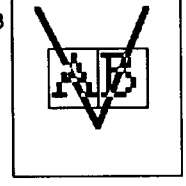


FIGURE 2b. SOURCE OR DESTINATION (77_{16})

Pattern	Source	Dest.	Funct.
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

MSB

LSB

Example

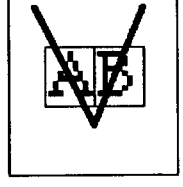


FIGURE 2c. SOURCE OVERLAY DESTINATION (33_{16})

Pattern	Source	Dest.	Funct.
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

MSB

LSB

Example

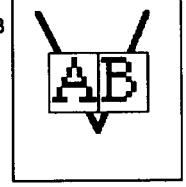


FIGURE 2d. SOURCE XOR DESTINATION OR PAT. ($6F_{16}$)

Pattern	Source	Dest.	Funct.
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

MSB

LSB

Example

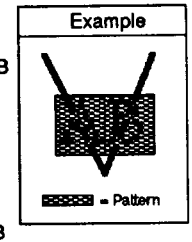


FIGURE 2e. SOURCE OR DESTINATION OR PAT. ($7F_{16}$)

Pattern	Source	Dest.	Funct.
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

MSB

LSB

Example

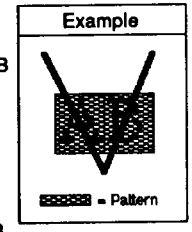


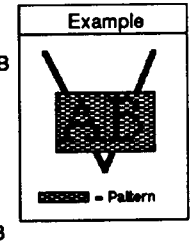
FIGURE 2f. SOURCE OVERLAY DEST. OR PAT. ($1F_{16}$)

Pattern	Source	Dest.	Funct.
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

MSB

LSB

Example



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.5 V to +7.0 V
Input Voltage	-0.5 V to +7.0 V
Output Voltage	-0.5 V to +7.0 V
Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Lead Temperature (10 s.)	300°C
Junction Temperature	175°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device under these or any other conditions above those listed in this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device

DC CHARACTERISTICS TA= 0°C to +70°C, VCC= 5 V ±0.25 V

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
VIH	High-Level Input Voltage		2.4			V	
VIL	Low-Level Input Voltage			0.6		V	
VOH	High-Level Output Voltage		2.4			V	VCC= Min; IOH= -400 µA
VOL	Low-Level Output Voltage			0.3	0.45	V	VCC= Min; IOL= 4.4 mA
IOH	High-Level Output Current		-400			µA	
IOL	Low-Level Output Current		4.4			mA	
IIL	Input Leakage Current				10	µA	VI = 0.45 V
II/O	I/O Leakage Current	0.7 V < Vo < Vcc			20	µA	
		0.4 V < Vo < Vcc		100			
ICC	Power Supply Current at DC				120	mA	VCC= Max

CAPACITANCE TA= 0°C to +70°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CI/O	I/O Capacitance			15	pF	
CI	Input Capacitance		6	15	pF	

AC TIMING CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ± 0.25 V

Symbol	Parameter	Min	Max	Unit	Conditions
tCSH	–CS, A0-A3 Hold After –WR Active	20		ns	
tRWW	–WR, –RD Signal Width	60		ns	
tCSS	–CS, A0-A3 Setup to –WR Inactive	0		ns	
CSV	Data Valid After –CS Active		120	ns	
tRDV	Data Valid After –RD Active		120	ns	
tRDH	Data Valid After –RD, –CS Inactive	5		ns	
tWRS	Data Setup to –WR Inactive	50		ns	
tWRH	Data Hold After –WR Inactive	30		ns	
tLSW	–LSSTB Pulse Width	60		ns	
tNLS	Time Between –LSSTB Pulses	0		ns	
tSDV	–LSSTB Inactive to Valid Data		120	ns	
LSF	–LSSTB Inactive to AOstb Active	30		ns	
tLDV	–LSSTB Active to Valid Data		170	ns	
tLDW	–LDSTB Pulse Width	60		ns	
tNLD	Time Between –LDSTB Pulses	150		ns	
tLDF	–LDSTB Inactive to –AOSTB Active	20		ns	
tLSS	Data Setup to –LSSTB Inactive	20		ns	
tLSH	Data Hold after –LSSTB Inactive	25		ns	
tLDS	Data Setup to –LDSTB Inactive	30		ns	
tLDH	Data Hold After –LDSTB Inactive			ns	
tFOV	Data Valid After –AOSTB Active		90	ns	
tDDV	Data Valid After Valid –LDSTB Data		140	ns	
tFDV	Bus High-Impedence After –AOSTB Inactive		40	ns	

FIGURE 3. REGISTER READ/WRITE TIMING

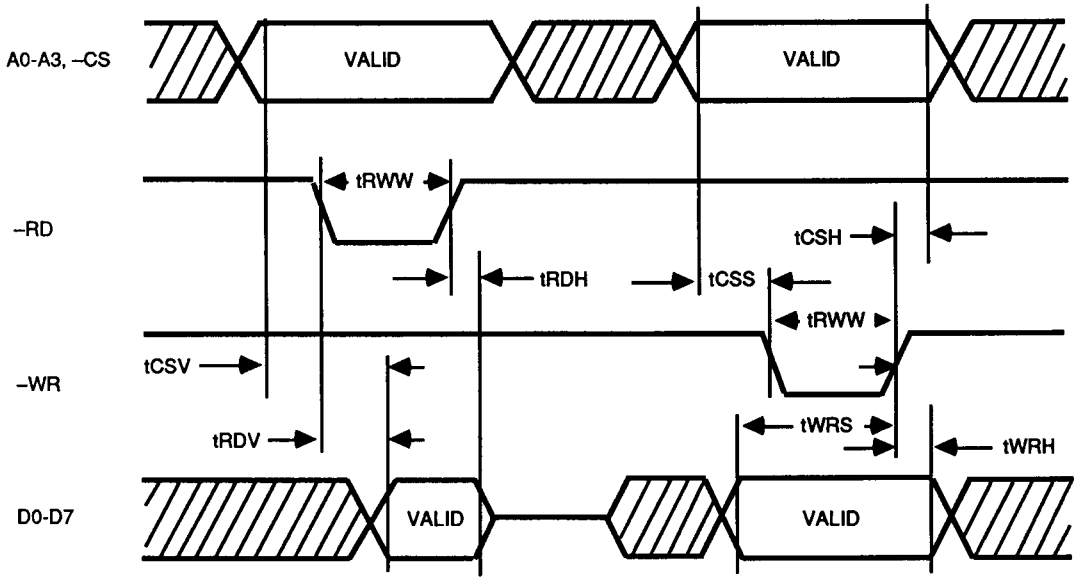


FIGURE 4. SOURCE REGISTER AND ALU OUTPUT CONTROL SIGNAL TIMING

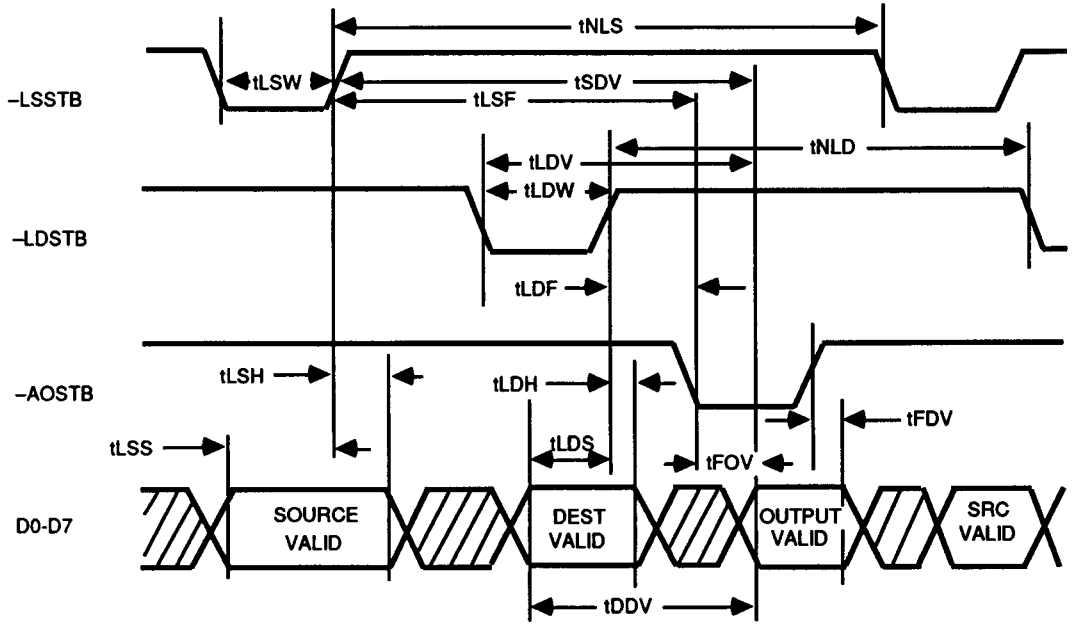


FIGURE 5. TYPICAL APPLICATION