Chris: it seems impossible to completely reformat this text to 70 columns for the ST shell :-((

THE AUTHORITATIVE GUIDE TO THE FALCON VIDEO HARDWARE

BY AURA AND ANIMAL MINE

[translator's note: This is the English translation of the excellent German document on the Falcon video registers by the members of Aura and Animal Mine. It was completed about 2 years ago, but I have only just received permission from Aura to publish the translation - thanks BDC! - so here it is at last. The ASCII version should be available on the disk itself for reference use. It has been reformatted to 72 columns to allow viewing on the ST shell (!) except in places where such formatting is not possible.

Incidentally, this document is for serious code-heads only. Ituses several dozen acronyms, so it's a good idea to have a pen and paper handy when reading!]

V I D E O - R E G I S T E R S

```
$FFFF8200 [R/W] ********
$FFFF8201 [R/W] 76543210  ............................. VIDEO-BASE HI
                      [ Writing to this clears Video-Address Lo-Byte ]
$FFFF8202 [R/W] ********
$FFFF8203 [R/W] 76543210 ............................. VIDEO-BASE MI
                      [ Writing to this clears Video-Address Lo-Byte ]
$FFFF8204 [R/W] ********
$FFFF8205 [R/W] 76543210  .................. VIDEO-ADDRESS-COUNTER HI
$FFFF8206 [R/W] ********
$FFFF8207 [R/W] 76543210  .................. VIDEO-ADDRESS-COUNTER MI
$FFFF8208 [R/W] ********
$FFFF8209 [R/W] 76543210  .................. VIDEO-ADDRESS-COUNTER LO
$FFFF820A [R/W] _______0  ................................. SYNC-MODE
                      ||
                      |+--Synchronisation [ 0:internal / 1:external ]
                      +---Vertical frequency [ Read-only bit ]
                          [ Monochrome monitor:0 / Colour monitor:1 ]
$FFFF820B [R/W] ________
$FFFF820C [R/W] ********
$FFFF820D [R/W] 7654321_  ............................. VIDEO-BASE LO
                     Video address must be a multiple of four in
                     bitplane modes
$FFFF820E [R/W] _______0  ............................ LINE-OFFSET HI
$FFFF820F [R/W] 76543210  ........................................ LO
                      [ Line-Offset measured in words! ]
$FFFF8210 [R/W] ______10  ............................ LINE-WIDTH HI
$FFFF8211 [R/W] 76543210  .....................................LO
                      [ Line-Width measured in words! ]
$FFFF8212 [R/W] ********
$FFFF8213 [R/W] ********
$FFFF8214 [R/W] ********
$FFFF8215 [R/W] ********
$FFFF8216 [R/W] ********
$FFFF8217 [R/W] ********
$FFFF8218 [R/W] ********
$FFFF8219 [R/W] ********
$FFFF821A [R/W] ________
```

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$FFFF821B [R/W] ________
$FFFF821C [R/W] ********
$FFFF821D [R/W] ********
$FFFF821E [R/W] ********
$FFFF821F [R/W] ********
$FFFF8220 [R/W] ********
$FFFF8221 [R/W] ********
$FFFF8222 [R/W] ********
$FFFF8223 [R/W] ********
$FFFF8224 [R/W] ********
$FFFF8225 [R/W] ********
$FFFF8226 [R/W] ********
$FFFF8227 [R/W] ********
$FFFF8228 [R/W] ********
$FFFF8229 [R/W] ********
$FFFF822A [R/W] ________
$FFFF822B [R/W] ________
$FFFF822C [R/W] ********
$FFFF822D [R/W] ********
$FFFF822E [R/W] ********
$FFFF822F [R/W] ********
$FFFF8230 [R/W] ********
$FFFF8231 [R/W] ********
$FFFF8232 [R/W] ********
$FFFF8233 [R/W] ********
$FFFF8234 [R/W] ********
$FFFF8235 [R/W] ********
$FFFF8236 [R/W] ********
$FFFF8237 [R/W] ********
$FFFF8238 [R/W] ********
$FFFF8239 [R/W] ********
$FFFF823A [R/W] ________
$FFFF823B [R/W] ________
$FFFF823C [R/W] ********
$FFFF823D [R/W] ********
$FFFF823E [R/W] ********
$FFFF823F [R/W] ********
$FFFF8240 [R/W] ____3210  ..............................ST COLOR $00 HI
                    ||||
                    ++++--Red intensity [ Order of bits : 0321 ]
$FFFF8241 [R/W] 76543210  ..............................ST COLOR $00 LO
                ||||||||
                ||||++++--Blue intensity [ Order of bits : 0321 ]
                ++++------Green intensity [ Order of bits: 0321 ]
$FFFF8242 [R/W] ____3210  ..............................ST COLOR $01 HI
$FFFF8243 [R/W] 76543210  ..............................LO
$FFFF8244 [R/W] ____3210  ..............................ST COLOR $02 HI
$FFFF8245 [R/W] 76543210  ..............................LO
$FFFF8246 [R/W] ____3210  ..............................ST COLOR $03 HI
$FFFF8247 [R/W] 76543210  ..............................LO
$FFFF8248 [R/W] ____3210  ..............................ST COLOR $04 HI
$FFFF8249 [R/W] 76543210  ..............................LO
$FFFF824A [R/W] ____3210  ..............................ST COLOR $05 HI
$FFFF824B [R/W] 76543210  ..............................LO
$FFFF824C [R/W] ____3210  ..............................ST COLOR $06 HI
$FFFF824D [R/W] 76543210  ..............................LO
$FFFF824E [R/W] ____3210  ..............................ST COLOR $07 HI
$FFFF824F [R/W] 76543210  ..............................LO
$FFFF8250 [R/W] ____3210  ..............................ST COLOR $08 HI
$FFFF8251 [R/W] 76543210  ..............................LO
$FFFF8252 [R/W] ____3210  ..............................ST COLOR $09 HI
$FFFF8253 [R/W] 76543210  ..............................LO
$FFFF8254 [R/W] ____3210  ..............................ST COLOR $0A HI
$FFFF8255 [R/W] 76543210  ..............................LO
$FFFF8256 [R/W] ____3210  ..............................ST COLOR $0B HI
$FFFF8257 [R/W] 76543210  ..............................LO
```

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$FFFF8258 [R/W] ____3210  ........................... ST COLOR $0C HI
$FFFF8259 [R/W] 76543210  .........................................LO
$FFFF825A [R/W] ____3210  ........................... ST COLOR $0D HI
$FFFF825B [R/W] 76543210  .........................................LO
$FFFF825C [R/W] ____3210  ........................... ST COLOR $0E HI
$FFFF825D [R/W] 76543210  .........................................LO
$FFFF825E [R/W] ____3210  ........................... ST COLOR $0F HI
$FFFF825F [R/W] 76543210  .........................................LO
$FFFF8260 [R/W] ______10  ............................. ST-SHIFT-MODE
                  ||  [ Writing to this alters Line-Width and
                  ||                              Video Control ]
                  ||  Video-Mode Control Bits:      <>%10   =%10
                  ||                          $FF8210 $FF82C2 $FF82C2
                  00--4 planes/320 Pixels=> $0050   $0000   $0005
                  01--2 planes/640 Pixels=> $0050   $0004   $0009
                  10--1 plane /640 Pixels=> $0028   $0006   $0008
                  11--? Resrvd/320 Pixels=> $0050   $0000   $0000
                      [ Writing to this can turn on STe modes: if
                      Bits 10/8/4 of FALCON-SHIFT=0, STE-Palette
                      is selected and Base Offset is raised to 64
                      video-clock cycles. ]
$FFFF8261 [R/W] ________
$FFFF8262 [R/W] ________
$FFFF8263 [R/W] ________
$FFFF8264 [R/W] ________  ................................ H-SCROLL HI
                  ||||  [ Shadow register for $FFFF8265 ]
                  ++++--Pixel shift [ 0:normal / 1..15:Left shift ]
                      [ Change in line-width NOT required ]
$FFFF8265 [R/W] ____3210  ................................H-SCROLL LO
                  ||||
                  ++++--Pixel [ 0:normal / 1..15:Left shift ]
                      [ Change in line-width NOT required ]
$FFFF8266 [R/W] _____210  ....................... FALCON-SHIFT-MODE HI
                   |||
                   ||+--True Colour mode [ 0:Off / 1:On ]
                   |+---Overlay mode [ 0:Off / 1:On ]
                   +----Monochrome 2-colour [ 0:Off / 1:On ]
$FFFF8267 [R/W] 76543210  ....................... FALCON-SHIFT-MODE LO
                |||||||
                ||||++++--16-Colour Bank for Falcon mode
                ||||      0-15: Colour bank choice from 256-colour
                ||||            table in 16 colour multiples
                |||+------8 Bitplane mode [ 0:Off / 1:On ]
                ||+-------Vertical sync [ 0:internal / 1:external ]
                |+--------Horizontal sync [ 0:internal / 1:external ]
                +---------??Unused??
                          [ Writing to this switches on FALCON modes
                            and Falcon palette is switched on. If
                            Bits 10/8/4=0 then 16-colour mode
                            activated ]

$FFFF8268 [R/W] ________
$FFFF8269 [R/W] ________
$FFFF826A [R/W] ________
$FFFF826B [R/W] ________
$FFFF826C [R/W] ________
$FFFF826D [R/W] ________
$FFFF826E [R/W] ________
$FFFF826F [R/W] ________
$FFFF8270 [R/W] ________
$FFFF8271 [R/W] ________
$FFFF8272 [R/W] ________
$FFFF8273 [R/W] ________
$FFFF8274 [R/W] ________
$FFFF8275 [R/W] ________
$FFFF8276 [R/W] ________
```

```
$FFFF8277 [R/W] ________
$FFFF8278 [R/W] ________
$FFFF8279 [R/W] ________
$FFFF827A [R/W] ________
$FFFF827B [R/W] ________
$FFFF827C [R/W] ________
$FFFF827D [R/W] ________
$FFFF827E [R/W] ________
$FFFF827F [R/W] ________
$FFFF8280 [R/W] _______0  ................. HORIZONTAL-HOLD-COUNTER HI
$FFFF8281 [R/W] 76543210  ..................................... LO
                          [ Write access has no effect ]
$FFFF8282 [R/W] _______0  ................... HORIZONTAL-HOLD-TIMER HI
$FFFF8283 [R/W] 76543210  ..................................... LO
$FFFF8284 [R/W] _______0  ................. HORIZONTAL-BORDER-BEGIN HI
$FFFF8285 [R/W] 76543210  ..................................... LO
$FFFF8286 [R/W] _______0  ................... HORIZONTAL-BORDER-END HI
$FFFF8287 [R/W] 76543210  ..................................... LO
$FFFF8288 [R/W] ______10  ................. HORIZONTAL-DISPLAY-BEGIN HI
                        |
                        +-----HDB offset: graphic display begins in the
                              0: 1st Half-line
                              1: 2nd Half-line
$FFFF8289 [R/W] 76543210  ..................................... LO
$FFFF828A [R/W] _______0  ................... HORIZONTAL-DISPLAY-END HI
$FFFF828B [R/W] 76543210  ..................................... LO
$FFFF828C [R/W] _______0  ................... HORIZONTAL-SYNC-START HI
$FFFF828D [R/W] 76543210  ..................................... LO
$FFFF828E [R/W] _______0  ........................... HORIZONTAL-FS HI
$FFFF828F [R/W] 76543210  ..................................... LO
                          if Video-Control Bit 4 = 1:
                          Controls for how long the Hysnc impulses of
                          the previous half-line should be held after
                          the next half-line starts (affects only the
                          middle 5 HSync impulses.) Otherwise no
                          ascertainable function as yet. [See below
                          for explanation]


$FFFF8290 [R/W] _______0  ........................... HORIZONTAL-EE HI
$FFFF8291 [R/W] 76543210  ..................................... LO
                          if Video-Control Bit 4 = 1:
                          (see above), but only affects the first and
                          last 5 HSync impulses. Otherwise no
                          ascertainable function as yet.
$FFFF8292 [R/W] ________
$FFFF8293 [R/W] ________
$FFFF8294 [R/W] ________
$FFFF8295 [R/W] ________
$FFFF8296 [R/W] ________
$FFFF8297 [R/W] ________
$FFFF8298 [R/W] ________
$FFFF8299 [R/W] ________
$FFFF829A [R/W] ________
$FFFF829B [R/W] ________
$FFFF829C [R/W] ________
$FFFF829D [R/W] ________
$FFFF829E [R/W] ________
$FFFF829F [R/W] ________
$FFFF82A0 [R/W] _____210  .............. VERTICAL-FREQUENCY-COUNTER HI
$FFFF82A1 [R/W] 76543210  ..................................... LO
                          [ Write access has no effect ]
$FFFF82A2 [R/W] _____210  ................. VERTICAL-FREQUENCY-TIMER HI
$FFFF82A3 [R/W] 76543210  ..................................... LO
$FFFF82A4 [R/W] _____210  ................... VERTICAL-BORDER-BEGIN HI
$FFFF82A5 [R/W] 76543210  ..................................... LO
```

```
$FFFF82A6 [R/W] _____210  ..................... VERTICAL-BORDER-END HI
$FFFF82A7 [R/W] 76543210  ........................................... LO
$FFFF82A8 [R/W] _____210  ................... VERTICAL-DISPLAY-BEGIN HI
$FFFF82A9 [R/W] 76543210  ........................................... LO
$FFFF82AA [R/W] _____210  ..................... VERTICAL-DISPLAY-END HI
$FFFF82AB [R/W] 76543210  ........................................... LO
$FFFF82AC [R/W] _____210  ..................... VERTICAL-SYNC-START HI
$FFFF82AD [R/W] 76543210  ........................................... LO
$FFFF82AE [R/W] ________
$FFFF82AF [R/W] ________
$FFFF82B0 [R/W] ________
$FFFF82B1 [R/W] ________
$FFFF82B2 [R/W] ________
$FFFF82B3 [R/W] ________
$FFFF82B4 [R/W] ________
$FFFF82B5 [R/W] ________
$FFFF82B6 [R/W] ________
$FFFF82B7 [R/W] ________
$FFFF82B8 [R/W] ________
$FFFF82B9 [R/W] ________
$FFFF82BA [R/W] ________
$FFFF82BB [R/W] ________
$FFFF82BC [R/W] ________
$FFFF82BD [R/W] ________
$FFFF82BE [R/W] ________
$FFFF82BF [R/W] ________
$FFFF82C0 [R/W] _______0  ........................... VIDEO-CONTROL HI
                        |
                        +--Horizontal Base Offset:
                              0: 128 Video cycles
                              1: 64 Video cycles
$FFFF82C1 [R/W] 76543210  ........................... VIDEO-CONTROL LO
                |||||||  Video mode control bits
                |||||||  Bits 0 & 1 set as $FFFF8006 Bits 6 & 7
                ||||||00--Monochrome monitor [ SM124 ]
                ||||||01--Colour monitor [ SC1224 und SC1435 ]
                ||||||10--VGA monitor
                ||||||11--TV set
                |||||+---Video base clock: 0: 32MHz/1: 25.175MHz
                |||||
                ||||+---15 Halfline-HSyncs from start of bottom
                ||||      border [ 0:Off / 1:On ]
                |||+----??Unknown??
                ||+-----VSync-switch: 0:neg've(5V>0V)/ 1:pos've(0V>5V)
                |+------HSync-switch: 0:neg've(5V>0V)/ 1:pos've(0V>5V)
                +-------Video data-bus width: 0:16 Bits/ 1:32 Bits
                          Falcon030 has a *32* Bit Video data-bus

$FFFF82C2 [R/W] ________  ............................. VIDEO-MODE HI
$FFFF82C3 [R/W] ____3210  ........................................... LO
                    ||||
                    |||+--Double Line mode [ 0:Off / 1:On ]
                    ||+---Interlace [ 0:Off / 1:On ]
                    ||
                    ||    Sets Video divider AND Cycles/pixel:
                    ||    - Video system divider in Falcon mode
                    ||      when Video-Mode-Control bits = %10 (VGA):
                   00----4
                   01----2
                   10----2
                   11----n/a (Video system not clocked)
                   ||      For all other Video-Mode-Control values:
                   00----4
                   01----2
                   10----1
                   11----n/a
```

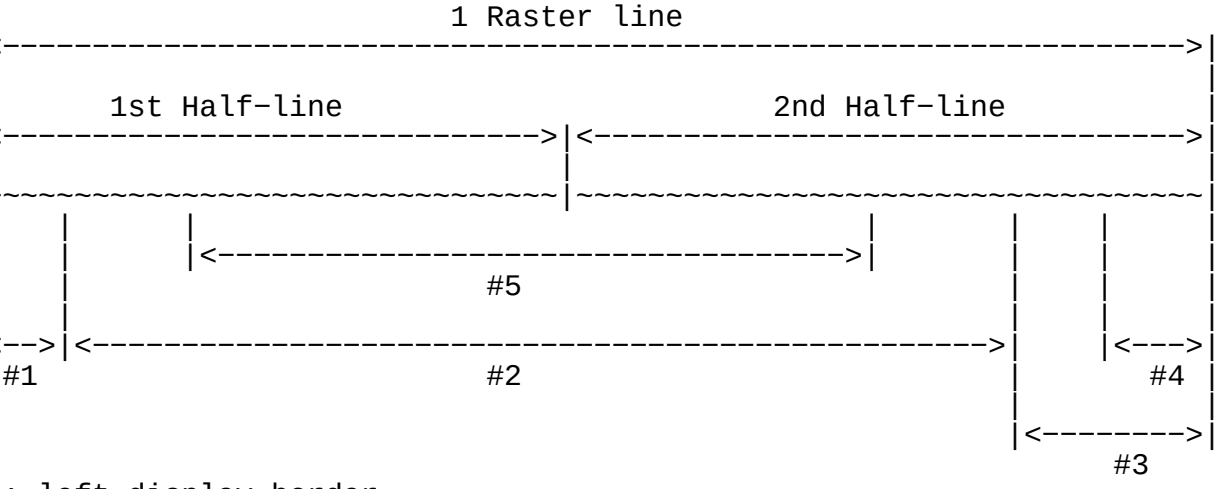
```
                    ||      For STE Compatibility mode,no matter what
                    ||      Video-Mode-Control-Bits are set:
                   00----16
                   01----16
                   10----16
                   11----n/a
                    ||
                    ||    - Pixel cycle-length: (i.e. cycles/pixel)
                   00----4 cycles long
                   01----2 cycles long
                   10----1 cycle long
                   11----n/a

*****************************************************************
                 2 5 6   C O L O R     R E G I S T E R S
*****************************************************************

$FFFF9800 [R/W] :$FC 765432__ ............... FALCON-COLOR $00  Red
                     ||||||
                     ++++++------ 0-63: Red Brightness
$FFFF9801 [R/W] :$FC 765432__ ............... FALCON-COLOR $00 Green
                     ||||||
                     ++++++------ 0-63: Green Brightness
$FFFF9802 [R/W] :$00 ******
$FFFF9803 [R/W] :$00 765432__ ............... FALCON-COLOR $00  Blue
                     ||||||
                     ++++++------ 0-63: Blue Brightness
    :       :     :    :
    :       :     :    :
    :       :     :    :
$FFFF9BFC [R/W] :$00 765432__ ................ FALCON-COLOR $FF  Red
$FFFF9BFD [R/W] :$00 765432__ ................ FALCON-COLOR $FF Green
$FFFF9BFE [R/W] :$00 ******
$FFFF9BFF [R/W] :$00 765432__ ................ FALCON-COLOR $FF Blue


-------------------------------------------------------------------------
-------------------------------------------------------------------------
Video System Standard Values in RGB and TV mode, 50 Hz:

       FALCON VIDEOREGISTERS $82xx.w:  (All hexadecimal word values!)
MODE   | 10| 60| 66| 82| 84| 86| 88| 8A| 8C| A2| A4| A6| A8| AA| AC| C0| C2
-------------------------------------------------------------------------
ST-LOW: 050 000 000 03E 032 009 23F 01C 034 271 265 02F 06F 1FF 26B 081 000
ST-MED: 050 010 000 03E 032 009 23F 01C 034 271 265 02F 06F 1FF 26B 081 004
ST-HIG: 028 0x0 400 1FE 199 050 3EF 0A0 1B2 270 265 02F 07E 20E 26B 181 006
  2/80: 028 0x0 400 1FE 199 050 3EF 0A0 1B2 271 265 02F 07F 20F 26B 181 004
  4/40: 028 010 000 03E 030 008 239 012 034 271 265 02F 07F 20F 26B 181 000
  4/80: 050 010 000 03E 030 008 002 020 034 271 265 02F 07F 20F 26B 181 004
 16/40: 050 0x0 000 0FE 0CB 027 00C 06D 0D8 271 265 02F 07F 20F 26B 181 000
 16/80: 0A0 0x0 000 1FE 199 050 04D 0FE 1B2 271 265 02F 07F 20F 26B 181 004
256/40: 0A0 0x0 010 0FE 0CB 027 01C 07D 0D8 271 265 02F 07F 20F 26B 181 000
256/80: 140 0x0 010 1FE 199 050 05D 10E 1B2 271 265 02F 07F 20F 26B 181 004
TRU/40: 140 0x0 100 0FE 0CB 027 02E 08F 0D8 271 265 02F 07F 20F 26B 181 000
TRU/80: 280 0x0 100 1FE 199 050 071 122 1B2 271 265 02F 07F 20F 26B 181 004
+ INTERLACE:                                -1         -1 -1         +2


MODE DESCRIPTIONS: Compatibility mode or 'colours/column'

(WARNING!  ST-High Values are already interlaced on RGBs!)

-------------------------------------------------------------------------
Video System Standard Values in VGA Modes, 60 Hz (59.58 Hz on Falcon):
(Double-Line on)
```

```
       FALCON VIDEO-REGISTERS $82xx.w:  (All hexadecimal word values)
MODE   | 10| 60| 66| 82| 84| 86| 88| 8A| 8C| A2| A4| A6| A8| AA| AC| C0| C2
-------------------------------------------------------------------------
ST-LOW: 050 000 000 017 012 001 20E 00D 011 419 3AF 08F 08F 3AF 415 186 005
ST-MED: 050 010 000 017 012 001 20E 00D 011 419 3AF 08F 08F 3AF 415 186 009
ST-HIG: 028 0x0 400 0C6 08D 015 273 050 096 419 3AF 08F 08F 3AF 415 186 008
  2/80: 028 0x0 400 0C6 08D 015 273 050 096 419 3FF 03F 03F 3FF 415 186 009
  4/40: 028 010 000 017 012 001 20A 009 011 419 3FF 03F 03F 3FF 415 186 005
  4/80: 050 010 000 017 012 001 20E 00D 011 419 3FF 03F 03F 3FF 415 186 009
 16/40: 050 0x0 000 0C6 08D 015 28A 06B 096 419 3FF 03F 03F 3FF 415 186 005
 16/80: 0A0 0x0 000 0C6 08D 015 2A3 07C 096 419 3FF 03F 03F 3FF 415 186 009
256/40: 0A0 0x0 010 0C6 08D 015 29A 07B 096 419 3FF 03F 03F 3FF 415 186 005
256/80: 140 0x0 010 0C6 08D 015 2AB 084 096 419 3FF 03F 03F 3FF 415 186 009
TRU/40: 140 0x0 100 0C6 08D 015 2AC 091 096 419 3FF 03F 03F 3FF 415 186 005
TRU/80: (officially impossible)

DOUBLE LINE OFF:                                                       -1

-------------------------------------------------------------------------
Video System Standard Values on SM 124, 71 Hz:

       FALCON VIDEO-REGISTERS $82xx.w:  (Allhexadecimal word values!)
MODE   | 10| 60| 66| 82| 84| 86| 88| 8A| 8C| A2| A4| A6| A8| AA| AC| C0| C2
-------------------------------------------------------------------------
ST-HIG: 028 020 000 01A 000 000 20F 00C 014 3E9 000 000 043 363 3E7 080 008
-------------------------------------------------------------------------
```

Caution: This documentation should not be seen as a reference work, but merely enables a brief introduction to the video system. All values were measured using an oscilloscope and confirmed by the operating system. There will however be differences between the values of OS-registers and my calculated values since the XBIOS may change some display control registers afterwards.

Horizontal Time-Setup:

Construction of screenlines:



#1: left display border
#2: visible screen area
#3: right display border
#4: HSync impulse
#5: graphic display area [area where screen data is translated to bitmaps]

Every raster line (even in the border area) is constructed in the following way: left border, visible area (with graphic display when

applicable), and finally the right border, with the Hsync impulses in the right border. Basically we can say that one line is divided into two half−lines: to be able to calculate the horizontal registers for the screen’s half−lines we need a few details:

− Video base clock: 32MHz, 25.175 MHz or external clock

	RGB/TV	VGA	Monochrome
− Monitor’s horizontal frequency:	15625 Hz	31467 Hz	35714 Hz
− Duration of Hsync impulse:	4.7us	3.81us	3.00 us
− Duration of right border:	6.2us	4.45us	0.00 us
− Duration of left border:	5.145us	1.91us	0.00 us

These values are used by the operating system. The duration of the Hsync impulse should not be changed, and the border duration should not be significantly reduced.

In the video system, the time setup is measured in clock−cycles . As a result a certain number of clock−cycles must elapse until (for example) the right border becomes active. The combined contents of the registers depends upon the above time settings (these can of course be altered, there are really no hard−and−fast values for the video system itself, apart from the requirements of the monitors), upon the video base clock and the video clock divider which divides the base frequency.

The video clock divider is set through Video−Mode ($82C2), bits 2/3, and is connected with the Video−Mode Control Bits (Video−Control bits 0/1) or via the STe compatibility mode. Important note: the video clock divider and cycles/pixel are _both_ controlled by bits 2/3 of Video−Mode.

First, to calculate the following horizontal registers:

HHT (Horizontal−Hold−Timer) defines the number of video cycles in a half−line:

$$HHT(\$8282) = int\left(\frac{\text{Video base frequency}}{\text{Horizontal frequency in Hz} * \text{Divider} * 2} - 2\right)$$

The Horizontal−Hold−Counter ($8280) is set up according to the HHT and counts the individual clock impulses up to the value of HHT. If the valueis exceeded, that is HHC = HHT+1, then the first half−line is finished andthe counter starts again from the beginning for the next half−line. In this way the HHT contains the number of clock cycles in a half−line.All following registers must lie with the values of HHT minus 1, sincethey contain the Video counter position at which an action (such asthe start of the left border etc.) is carried out.

HSS (Horizontal Sync Start) denotes at what video clock position in thesecond half−line the Hysnc impulse should be triggered, until the end of that half−line:

$$HSS(\$828A) = HHT + 1 - int\left(\frac{\text{HSyncduration in us} * \text{Video base clock}}{\text{Divider}}\right)$$

If HSS is greater than HHT+1 then no Vsync impulse is triggered.

HBB (Horizontal Border Begin) denotes at what video clock position in thesecond half−line the right border should be triggered, until the end of that half−line:

$$HBB(\$8284) = HHT + 1 - int\left(\frac{\text{rt bord duration in us} * \text{Video base clock}}{\text{Divider}}\right)$$

If HSS is greater than HHT+1 then no border is present.
If a monochrome monitor (e.g. SM124) is used then the HBB has no significance and no border is present.

HBE (Horizontal Border End) denotes the Video Counter position in the first half-line where the left border should cease being active:

```
                |left border duration in us * Video base clock |
HBE($8286) = int|----------------------------------------------|
                |                  Divider                     |
```

If HBE is greater than HHT+1 then a border is produced across both half-lines. If a monochrome monitor (e.g. SM124) is used then the HBE has no significance and no border is present.

Now for the interesting bit: the horizontal graphic display. I spent most of my time and a lot of effort on this part and isn't easy to understand.

The video system has a peculiar way of representing the horizontal graphic display. First of all we define in which half-line (first or second, according to bit 9 of the HDB-register $8288) the graphic display should be initiated. If this is defined then the video system waits in the chosen half-line until the contents of HHC reaches that of the HDB register ($8288) and then it starts the graphic display. Before this, though, the video system lies in a 'Wait state' (I've no idea why, perhaps to unburden the bus a bit or to load the first chunk of graphic data into the internal VIDEL-buffer.)

The length of this wait state can be worked out from the HDB-offset. The graphic display is not begun until after this is reached. The HDE (Horizontal Display End, $828A) then defines the right hand edge of the graphic display. This operates in the same way as described above; first the system waits until HHC has reached the value of the HDE register and again inserts a pause, to end the graphic display after this. The wait state's length can be worked out from the HDE-offset. In contrast to the HDB, the HDE can only be set in the second half-line.

Now for the offsets:

The wait-state which the video system inserts before the graphic display can be calculated from the HDB-offset. This offset is dependent upon the number of bitplanes and the chosen divider, as well as the pixel cycle-length which defines the resolution. However we draw a distinction between the bitplane and truecolour modes:

In Falcon bitplane mode:

```
              |         |8 Words*16 Pixels      |                |
              |Base Off+|----------------- +16+2| * Cycles/pixel |
              |         |  No. of planes        |                |
HDB-Offset=int|-----------------------------------------------| + 1
              |                    Divider                    |
```

In STe-compatible bitplane mode:

```
              |             |8 Words*16 Pixels   |                |
              |64+Base Off +|---------------- + 2| * Cycles/pixel |
              |             |  No. of planes     |                |
HDB-Offset=int|-----------------------------------------------|+1
              |                    Divider                    |
```

In Truecolour mode:

```
                |Base offset + 16 Pixels * Cycles/pixel |
```

```
HDB-Offset = int|--------------------------------------| + 1
               |                 Divider                |
```

The Base Offset is set in the Video-Control Register ($82C0) bit 8. When the bit is cleared then 128 cycles are taken as the Base Offset, 64 if the bit is set. If an STe-compatible mode is selected, which uses the STe palette, 64 must be added to the Base Offset - apparently for compatibility reasons.

The wait-state which the video system inserts before the graphic display can be calculated from the HDE-offset. This offset is also dependent upon the number of bitplanes and the chosen divider, as well as the pixel cycle-length, which defines the resolution. Here as well we must differentiate between bitplane and truecolour modes:

In Falcon and STE-compatible bitplane mode:

```
              ||8 Words*16 Pixels    |                |
              ||-----------------  + 2| * Cycles/pixel |
              ||  No. of planes      |                |
HDE-Offset=int|---------------------------------------|
              |                Divider                 |
```

In Truecolour mode:
HDE-Offset = 0

When calculating the HDB and HDE it should be noted, that the number of horizontal pixels cannot be defined arbitrarily, except in Truecolour mode. We can arrive at the allowed pixel multiple using the following formula:

$$\text{Horizontal pixel multiple} = \frac{8 \text{ Words} * 16 \text{ Pixels}}{\text{No. of planes}}$$

In truecolour mode a fine definition of 1 pixel is possible. In bitplane mode an incorrect setting of HDB and HBE leads to nice effects like the overlapping of planes or holes without any graphics.

An example:
Only pixel multiples of 128 are allowed in 2-colour mode. HDB/HBE must be set so that on the screen a multiple of of 128 pixels shown. This is why no 2-colour, 40 column mode is supported by the operating system, because 320 is not divisible by 128.

So, now to calculating the HDB and HBE:

Preamble: when discussing the video-system, we must get used to talking about 'cycles' and not 'pixels'. The number of pixels is given by cycles divided by cycles/pixel. So if we want a 32Mhz clock and a 4 cycles/pixel, then the theoretically possible number of pixels is 8000000. Often that is also indicated by a 'video bandwidth' of 8Mhz. So we assume that the graphic display should be started after 50 cycles and the graphic display should be 1280 cycles in length. Now we have a choice of 1,2 or 4 cycles/pixel or 1280,640 or 320 pixels. Now I shall choose to have 2 cycles/pixels and correspondingly have a display of 640 pixels. We must still take into account the clock divider which correponds to this, which in turn affects the bitplane and compatibility-modes.

I'll now choose the 16-colour Falcon mode and with this I MUST use a divider of 2, because the number of cycles/pixel AND the divider are represented by the same bits (see register $FF82C0.)

Now we can calculate the HDB offset (for the formula, see above.) Here we must be careful to use the formula for the Falcon video-modes.

Vertical Time Setup

Every screen setup is made built out of from half−lines. The number of half−lines is defined by the vertical frequency, in conjunction with the HHT which defines the duration of one half−line. If we have a horizontal frequency of 15625Hz, then 312.5 lines or 625 half−lines are needed to produce a vertical frequency of 50Hz. HHT of course MUST be set up so that a horizontal frequency of 15625Hz is produced (see above.)

Here again some monitor−dependent details will be necessary:

	TV/RGB	50HzTV/RGB	60HzVGA	SM124
− Monitor's Horizontal frequency:	15625 Hz	15625 Hz	31467 Hz	35714 Hz
− Monitor's Vertical frequency:	50 Hz	59.52 Hz	59.58 Hz	71.43 Hz
− Duration of VSync impulse:	0.192ms	0.192ms	0.064ms	0.029 ms
− Duration of top border:	1.504ms	0.700ms	1.008ms	0.000 ms
− Duration of bottom border:	0.384ms	0.384ms	0.416ms	0.000 ms

These values are also used by the OS. The Vsync impulse should not be changed and the borders not significantly reduced.
It should be noted that the video system in 60Hz is programmed for ~59.5Hz.

Now here are the calculations for the individual vertical registers:

VFT (Vertical Frequency Timer) defines the number of half−lines per VBL:

$$VFT(\$82A2) = int\left|\frac{\text{Horizontal frequency}}{\text{Vertical frequency}}\right| * 2\ (+1)$$

^^^−when not interlaced

The Half−line counter VFC($82A0) is set up according to the VFT and counts individual half−lines up to the value of VFT. The VFC is always incremented when the HHC exceeds the value of the HHT. When VFC reaches the value of the VFT, the screen setup is at an end and the counter begins again. The VFT affects all the following registers.
The value of VFT should always be an odd number, unless interlace mode is enabled. In this case VFT, VDB and VDE should always contain even values.

VSS (Vertical Sync Start) defines from which half−line the Vsync impulse should be triggered, until the screen end:

$$VSS(\$82AC) = VFT - int|\text{VSync−Time in ms} * \text{Horizontal frequency in Hz} * 2|$$

VBB (Vertical Border Begin) defines from which half−line the bottom border should be active, until the screen end:

$$VBB(\$82A4) = VFT - int|\text{bottom border dur. in ms} * \text{Horiz.freq.} * 2|$$

If a monochrome monitor is connected VDB has no significance and no border is displayed.

VBE (Vertical Border End) defines until which half−line the top border should be active, from the screen start:

$$VBE(\$82A6) = VFT - int|\text{bottom border time in ms} * \text{Horiz.freq.} * 2|$$

If a monochrome monitor (e.g. SM124) is connected VDB has no significance and no border is displayed.

Setup of graphic display area:
==============================

VDB (Vertical Display Begin) defines at which half-line the graphic display should begin:
VDB($82A8) = No. of lines * 2 (+ 1)
^^^------- when not in interlace mode
If VDB is greater than VFT then no graphic display occurs.
If VDB is greater than VDE then graphic display occurs from VDB to VFT. The VDE register is then ignored.

VDE defines at which half-line the graphic display should cease:
VDE($82AA) = No. of lines * 2 (+ 1)
^^^------- when not in interlace mode
If VDE is less than VDB then no graphic display occurs. [??????????]
If VDE is less than VDB then graphic display occurs from VDB to VFT. The VDE register is then ignored.

The number of graphic-display lines is calculated by halving (due to the half-lines) the difference between VDB and VDE.

Incidental remarks:
In Burst Mode, the video system reads 17 32-bit data words into the VIDEL's FIFO buffer. The system requires 4 cycles per burst-cycle.

When setting the Video-Mode-Control bits by writing to $FF8260 [ST-Shift], the registers $FF8210 and $FF82C2 are automatically set by the video sytem so that an ST-compatible mode is produced (see also reg. $FF8260.) The effects all depend upon what type of monitor is set in the Video-Control bits: the registers will be changed according to this.

Switching to 2-colour mode appears to confuse the video system. Often we find that although all the registers have been correctly set the visible graphic area is out of line or cut off. This can be prevented by the use of 'CLR.W $FFFF8266.W' before setting the resolution through the Falcon and STe-shift registers. This is also the reason why the operating system does not produce a similar lack of synchronisation.

##
######### research and documentation by AURA and A.M. ###############
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(Transl. by Steve Tattersall)